# ANALOG-DIGITAL CONVERSION

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# CHAPTER 6
# INTERFACING TO DATA CONVERTERS

## SECTION 6.1: DRIVING ADC ANALOG INPUTS
*Walt Kester*

### Introduction

Before considering the detailed issues involved in driving ADCs, some general comments about trends in modern data converters are in order. Data converter performance is first and foremost, and maintaining that performance in a system application is extremely important. In low frequency measurement applications (10-Hz bandwidth signals or lower), Σ-Δ ADCs with resolutions up to 24 bits are now quite common. These converters generally have automatic or factory calibration features to maintain required gain and offset accuracy. In higher frequency signal processing, ADCs must have wide dynamic range (low distortion and noise), high sampling frequencies, and generally excellent ac specifications.

In addition to sheer performance, other characteristics such as low power, single supply operation, low cost, and small surface mount packages also drive the data conversion market. These requirements result in a myriad of application problems because of reduced signal swings, increased sensitivity to noise, etc. As has been mentioned previously in Chapter 3, the analog input to a CMOS ADC is usually connected directly to a switched-capacitor sample-and-hold (SHA), which generates transient currents that must be buffered from the signal source. This can present quite a challenge when selecting a drive amplifier. On the other hand, high performance data converters fabricated on BiCMOS or complementary bipolar processes are more likely to have internal buffering, but generally have higher cost and power consumption than their CMOS counterparts. The general trends in data converters are summarized in Figure 6.1.

- **Higher sampling rates, higher resolution, excellent AC performance**
- **Single supply operation (e.g., +5V, +3V, +2.5V, +1.8V)**
- **Lower power, shutdown or sleep modes**
- **Smaller input/output signal swings**
- **Differential inputs/outputs**
- **Maximize usage of low cost foundry CMOS processes**
- **Small surface mount packages**

***Figure 6.1:*** *Some General Trends in Data Converters*

It should be clear by now that selecting an appropriate drive circuit for a data converter application is highly dependent on the particular converter under consideration. Generalizations are difficult, but some meaningful guidelines can be followed.

To begin with, one shouldn't necessarily assume that a driver amplifier is always required. Some converters have relatively benign inputs and are designed to interface directly to the signal source. In many applications, transformer drive may be preferable. Because there is practically no industry standardization regarding ADC input structures, each ADC must be carefully examined on its own merits before designing the input interface circuitry.

If an amplifier is required, a fundamental requirement is that it not degrade the dc or ac performance of the converter. One might assume that a careful reading of the op amp datasheets would assist in the selection process—simply lay the data converter and the op amp datasheets side by side, and compare each critical performance specification. It is true that this method will provide some degree of success; however in order to perform an accurate comparison, the op amp must be specified under the exact operating conditions required by the data converter application. Such factors as gain, gain setting resistor values, source impedance, output load, input and output signal amplitude, input and output common-mode (CM) level, power supply voltage, etc., all affect op amp performance to some degree.

It is highly unlikely that even a well written op amp datasheet will provide an exact match to the operating conditions required in the data converter application. Extrapolation of specified performance to fit the exact operating conditions can give erroneous results. Also, the op amp may be subjected to transient currents from the data converter, and the corresponding effects on op amp performance are rarely found on datasheets.

Converter datasheets themselves can be a good source for recommended op amps and other application circuits. However, this information can become obsolete when newer op amps are introduced after the converter's initial release.

Analog Devices offers a parametric search engine which facilitates part selection (see http://www.analog.com). For instance, the first search might be for minimum power supply voltage, e.g., +3 V. The next search might be for bandwidth, and further searches on relevant specifications will narrow the selection of op amps even further. While not necessarily suitable for the final selection, this process can narrow the search to a manageable number of amplifiers whose individual datasheets can be retrieved, then reviewed in detail before final selection. Figure 6.2 summarizes the overall selection process.

- Some ADCs (DACs) do not require special input drivers (output buffers)
- The amplifier / transformer should not degrade the performance of the ADC (DAC)
- AC specifications are usually the most important
  - Noise
  - Bandwidth
  - Distortion
  - Settling time from transient currents
- Selection based on op amp data sheet specifications difficult due to varying conditions in actual application circuit with ADC (DAC):
  - Power supply voltages
  - Signal range (differential and common-mode)
  - Loading (static and dynamic)
  - Gain and gain-setting resistor values
- Parametric search engines may be useful
- ADC (DAC) data sheets often recommend op amps but may not include newly released products

***Figure 6.2:*** *ADC Driver (DAC Buffer) Selection Criteria*

## Amplifer DC and AC Performance Considerations

As discussed above, the amplifier (if required) should not degrade the performance specifications of the data converter. Today, ac specifications are generally paramount—especially with high-speed data converters. Chapter 2 of this book has discussed ADC and DAC specifications in detail, but it is useful to summarize the popular converter dynamic performance specifications in Figure 6.3.

- Signal-to-Noise-and-Distortion Ratio (SINAD, or S/N +D)
- Effective Number of Bits (ENOB)
- Signal-to-Noise Ratio (SNR)
- Analog Bandwidth (Full-Power, Small-Signal)
- Harmonic Distortion
- Worst Harmonic
- Total Harmonic Distortion (THD)
- Total Harmonic Distortion Plus Noise (THD + N)
- Spurious Free Dynamic Range (SFDR)
- Two-Tone Intermodulation Distortion
- Multi-tone Intermodulation Distortion

***Figure 6.3:*** *Popular Converter Dynamic Performance Specifications*

For comparison, the fundamental op amp dc and ac specifications are summarized in Figure 6.4. Not all op amps will have these specifications, however they should certainly have most of them listed on the data sheet if the op amp is to be a serious contender for a high performance data converter application.

- **DC**
  - **Input/Output Signal Range**
  - **Offset, offset drift**
  - **Input bias current**
  - **Open loop gain**
  - **Integral linearity**
  - **1/f noise (voltage and current)**

- **AC (Highly application dependent!)**
  - **Wideband noise (voltage and current)**
  - **Small and Large Signal Bandwidth**
  - **Harmonic Distortion**
  - **Total Harmonic Distortion (THD)**
  - **Total Harmonic Distortion + Noise (THD + N)**
  - **Spurious Free Dynamic Range (SFDR)**
  - **Third Order Intermodulation Distortion**

***Figure 6.4:*** *Key DC and AC Op Amp Specifications for ADC/DAC Applications*

Regardless of the importance of the ac specifications, the fundamental dc specifications must not be overlooked—especially in light of the implications of low voltage single-supply operation so popular today. The allowable input and output signal range becomes critically important in single supply applications as illustrated in the fundamental application circuit shown in Figure 6.5.

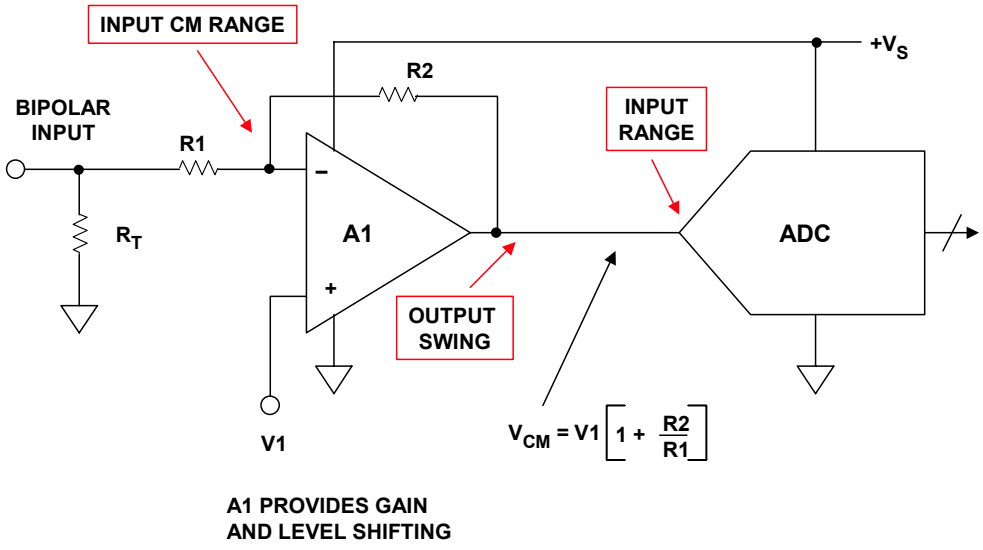



***Figure 6.5:*** *Input/Output Signal Swing and Common-Mode Range is Critical in Single-Supply ADC Driver Applications*

The circuit of Figure 6.5 shows an op amp as a simple dc-coupled single-supply ADC driver which provides the proper gain and level shifting for the bipolar (ground-referenced) input signal such that it matches the input range of the ADC. Several important points are illustrated in this popular circuit. The first consideration is the input range of the ADC, which in turn determines the output voltage swing requirement of the op amp. There are a number of single-supply CMOS ADCs with inputs that go from 0 V to the positive supply voltage. As will be illustrated shortly, even rail-to-rail output op amps cannot drive the signal completely to each rail. If, however, the ADC input range can be set so that the signal only goes to within a few hundred millivolts of each rail, then a single-supply "almost" rail-to-rail output op amp can often be used.

On the other hand, ADCs fabricated on BiCMOS or complementary bipolar processes typically have fixed input ranges that are usually at least several hundred millivolts from either rail, although many are not centered at the mid-supply voltage of $V_S/2$.

Equally important is the input common-mode voltage of the op amp. In the circuit of Figure 6.5, the input common-mode voltage is set by V1, which level shifts the amplifier output to the correct value. Obviously, V1 must lie within the input common-mode voltage range of the op amp in order for the circuit to work properly.

These restrictions can become quite severe when operating the entire circuit on a single low-voltage supply, and therefore a brief discussion of rail-to-rail op amps follows in order to better understand how to properly select the drive amplifier. We will discuss the input and output stage considerations separately.

**Rail-Rail Input Stages**

Today, there is common demand for op amps with input common-mode voltage that includes *both* supply rails, i.e., *rail-to-rail* common-mode operation. While such a feature is undoubtedly useful in some applications, engineers should recognize that there are still relatively few applications where it is absolutely essential. These applications should be distinguished from the many more applications where a common-mode input range *close* to the supplies, or one that includes *one* supply is necessary, but true input rail-to-rail operation is not.

In many single-supply applications, it is required that the input common-mode voltage range extend to one of the supply rails (usually ground). High-side or low-side current-sensing applications are typical examples of this. Many amplifiers can handle 0-V common-mode inputs, and they are easily designed using PNP differential pairs (or N-channel JFET pairs or PMOS pairs) as shown in Figure 6.6. The input common-mode range of such an op amp generally extends from about 200 mV below the negative rail ($-V_S$, or ground), to within 1 V to 2 V of the positive rail ($+V_S$).

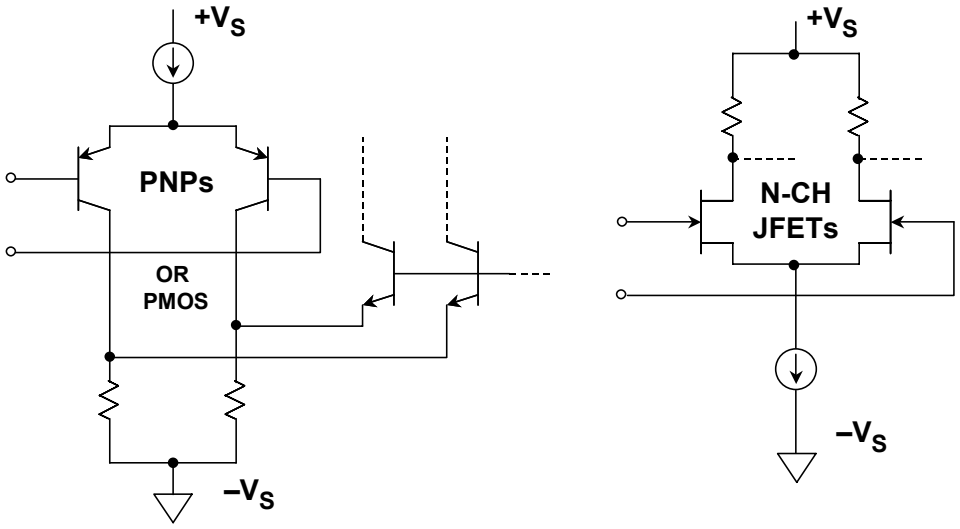



***Figure 6.6:*** *PNP, PMOS, or N-Channel JFET Stages Allow Common-Mode Inputs to Include the Negative Rail*

An input stage could also be designed with NPN transistors (or P-channel JFET pairs or NMOS pairs), in which case the input common-mode range would include the positive rail, and go to within about 1 V to 2 V of the negative rail. This requirement typically occurs in applications such as high-side current sensing.

A simplified diagram of what has become known as a true rail-to-rail input stage is shown in Figure 6.7. Note that this requires use of *two* long-tailed pairs, one of PNP bipolar transistors Q1-Q2, the other of NPN transistors Q3-Q4. Similar input stages can also be made with CMOS or JFET pairs.

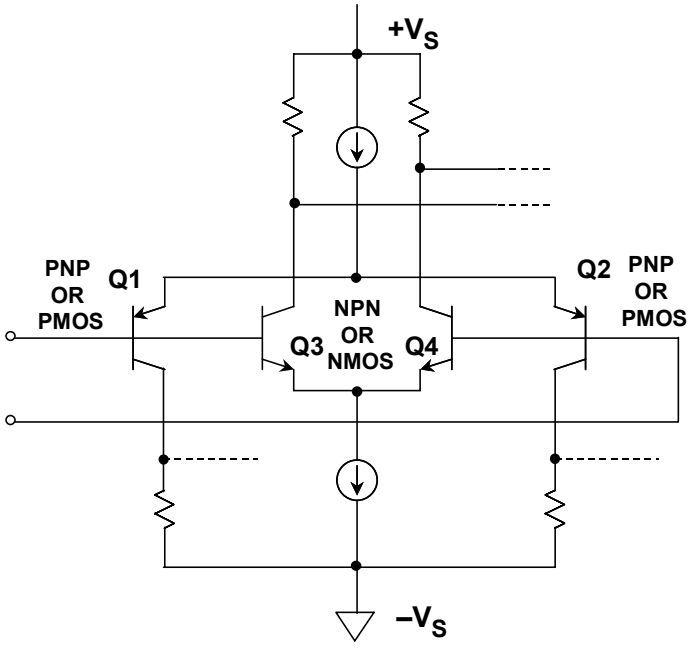



***Figure 6.7:*** *A True Rail-to-Rail Input Stage*

It should be noted that these two pairs will exhibit *different* offsets and bias currents, so when the applied common-mode voltage changes, the amplifier input offset voltage and input bias current does also. In fact, when both current sources remain active throughout most of the entire input common-mode range, amplifier input offset voltage is the *average* offset voltage of the two pairs. In those designs where the current sources are alternatively switched off at some point along the input common-mode voltage, amplifier input offset voltage is dominated by the PNP pair offset voltage for signals near the negative supply, and by the NPN pair offset voltage for signals near the positive supply. As noted, a true rail-to-rail input stage can also be constructed from CMOS transistors, for example as in the case of the CMOS AD8531/8532/8534 op amp family.

Amplifier input bias current, a function of transistor current gain, is also a function of the applied input common-mode voltage. The result is relatively poor common-mode rejection (CMR), and a changing common-mode input impedance over the common-mode input voltage range, compared to familiar dual-supply devices. These specifications should be considered carefully when choosing a rail-to-rail input op amp, especially for a non-inverting configuration. Input offset voltage, input bias current, and even CMR may be quite good over *part* of the common-mode range, but much worse in the region where operation shifts between the NPN and PNP devices, and vice versa.

True rail-to-rail amplifier input stage designs must transition from one differential pair to the other differential pair, somewhere along the input common-mode voltage range. Some devices like the OP191/291/491 family and the OP279 have a common-mode crossover threshold at approximately 1 V below the positive supply (where signals do not often occur). The PNP differential input stage is active from about 200 mV below the negative supply to within about 1 V of the positive supply. Over this common-mode range, amplifier input offset voltage, input bias current, CMR, input noise voltage/current are primarily determined by the characteristics of the PNP differential pair. At the crossover threshold, however, amplifier input offset voltage becomes the average offset voltage of the NPN/PNP pairs and can change rapidly.

Also, as noted previously, amplifier bias currents are dominated by the PNP differential pair over most of the input common-mode range, and change polarity and magnitude at the crossover threshold when the NPN differential pair becomes active.

Op amps like the OP184/284/484 family, utilize a rail-to-rail input stage design where both NPN and PNP transistor pairs are active throughout most of the entire input common-mode voltage range. With this approach to biasing, there is no common-mode crossover threshold. Amplifier input offset voltage is the average offset voltage of the NPN and the PNP stages, and offset voltage exhibits a smooth transition throughout the entire input common-mode range, due to careful laser trimming of input stage resistors.

In the same manner, through careful input stage current balancing and input transistor design, the OP184 family input bias currents also exhibit a smooth transition throughout the entire common-mode input voltage range. The exception occurs at the very extremes of the input range, where amplifier offset voltages and bias currents increase sharply, due to the slight forward-biasing of parasitic p-n junctions. This occurs for input voltages within approximately 1 V of either supply rail.

When *both* differential pairs are active throughout most of the entire input common-mode range, amplifier transient response is faster through the middle of the common-mode range by as much as a factor of 2 for bipolar input stages and by a factor of √2 for JFET input stages. This is due to the higher transconductance of two operating input stages.

The AD8027/8028 op amp family (Reference 1) has a pin-selectable crossover threshold which allows the user to choose the crossover point between the PNP/NPN input differential pairs. Depending upon the state of the *select* pin, the threshold can be set for 1.2 V from the positive rail (*select* pin open) or 1.2 V from the negative rail (*select* pin connected to positive supply voltage).

Input stage $g_m$ determines the slew rate and the unity-gain crossover frequency of the amplifier, hence response time degrades slightly at the extremes of the input common-mode range when either the PNP stage (signals approaching the positive supply rail) or the NPN stage (signals approaching the negative supply rail) are forced into cutoff. The thresholds at which the transconductance changes occur are approximately within 1 V of either supply rail, and the behavior is similar to that of the input bias currents.

In light of the many quirks of true rail-to-rail op amp input stages, applications which do require true rail-to-rail inputs should be carefully evaluated, and an amplifier chosen to ensure that its input offset voltage, input bias current, common-mode rejection, and noise (voltage and current) are suitable.

**Output Stages**

The earliest IC op amp output stages were NPN emitter followers with NPN current sources or resistive pull-downs, as shown in Figure 6.8A and B. Naturally, the slew rates were greater for positive-going than they were for negative-going signals.

While all modern op amps have push-pull output stages of some sort, many are still asymmetrical, and have a greater slew rate in one direction than the other. Asymmetry tends to introduce distortion on ac signals and generally results from the use of IC processes with faster NPN than PNP transistors. It may also result in an ability of the output to approach one supply more closely than the other in terms of saturation voltage.

In many applications, the output is required to swing only to one rail, usually the negative rail (i.e., ground in single-supply systems). A pulldown resistor to the negative rail will allow the output to approach that rail (provided the load impedance is high enough, or is also grounded to that rail), but only slowly. Using an FET current source instead of a resistor can speed things up, but this adds complexity, as shown in Fig. 6.8B.

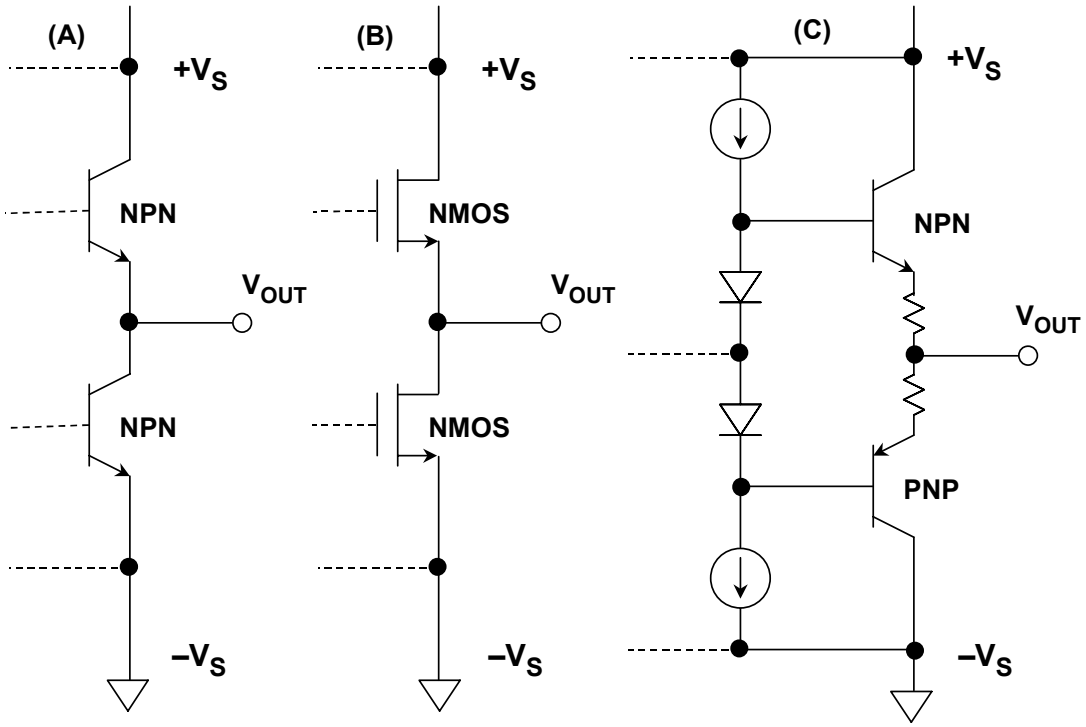



***Figure 6.8:*** *Some traditional Op Amp Output Stages*

With modern complementary bipolar (CB) processes, well matched high speed PNP and NPN transistors are readily available. The complementary emitter follower output stage shown in Fig. 6.8C has many advantages, but the most outstanding one is the low output impedance. However, the output voltage of this stage can only swing within about one $V_{BE}$ drop of either rail. Therefore, a usable output voltage range of +1 V to +4 V is typical of such a stage, when operated on a single +5-V supply.

The complementary common-emitter/common-source output stages shown in Figure 6.9A and B allow the op amp output voltage to swing much closer to the rails, but these stages have much higher open-loop output impedance than do the emitter follower-based stages of Fig. 6.8C

In practice, however, the amplifier's high open-loop gain and the applied feedback can still produce an application with low output impedance (particularly at frequencies below 10 Hz). What should be carefully evaluated with this type of output stage is the loop gain within the application, with the load in place. Typically, the op amp will be specified for a minimum gain with a load resistance of 10 kΩ (or more). Care should be taken that the application loading doesn't drop lower than the rated load, or gain accuracy may be lost.

It should also be noted these output stages can cause the op amp to be more sensitive to capacitive loading than the emitter-follower type. Again, this will be noted on the device data sheet, which will indicate a maximum of capacitive loading before overshoot or instability will be noted.

The complementary common emitter output stage using BJTs (Fig. 6.9A) cannot swing completely to the rails, but only to within the transistor saturation voltage ($V_{CESAT}$) of the rails. For small amounts of load current (less than 100 µA), the saturation voltage may be as low as 5 to 10 mV, but for higher load currents, the saturation voltage can increase to several hundred mV (for example, 500 mV at 50 mA).

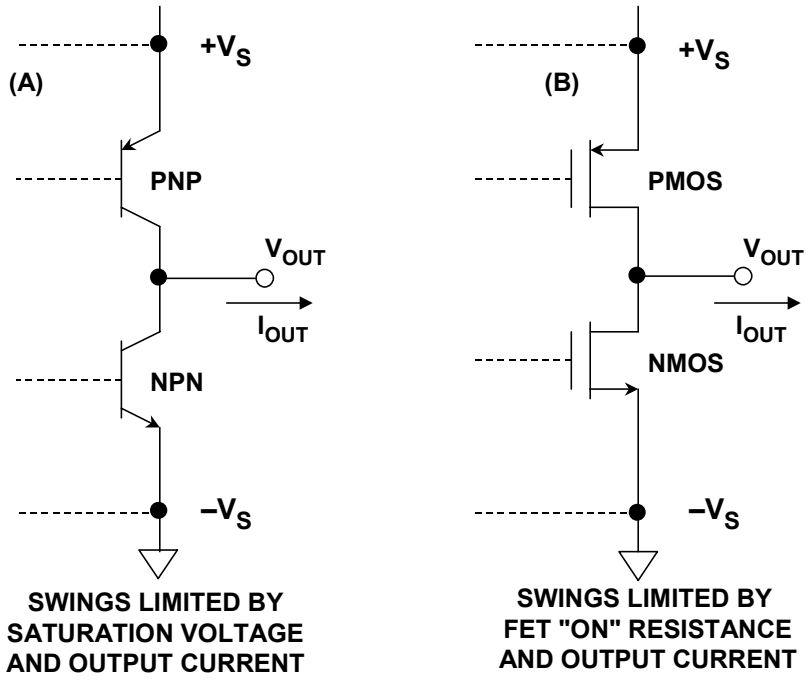



***Figure 6.9:*** *"Almost" Rail-To-Rail Output Stages*

On the other hand, an output stage constructed of CMOS FETs (Fig. 6.9B) can provide nearly true rail-to-rail performance, but only under no-load conditions. If the op amp output must source or sink substantial current, the output voltage swing will be reduced by the I×R drop across the FET's internal "on" resistance. Typically this resistance will be on the order of 100 Ω for precision amplifiers, but it can be less than 10 Ω for high current drive CMOS amplifiers.

For the above basic reasons, it should be apparent that there is no such thing as a *true* rail-to-rail output stage, hence the caption of Fig. 6.9 ("Almost" Rail-to-Rail Output Stages). The best any op amp output stage can do is an "almost" rail-to-rail swing, when it is lightly loaded.

**Gain and Level-Shifting Circuits Using Op Amps**

In dc-coupled applications, the drive amplifier must provide the required gain and offset voltage, to match the signal to the input voltage range of the ADC. Figure 6.10 summarizes various op amp gain and level shifting options. The circuit of Figure 6.10A operates in the non-inverting mode, and uses a low impedance reference voltage, $V_{REF}$, to offset the output. Gain and offset interact according to the equation:

$$V_{OUT} = [1 + (R2/R1)] \bullet V_{IN} - [(R2/R1) \bullet V_{REF}] \qquad \text{Eq. 6.1}$$

The circuit in Figure 6.10B operates in the inverting mode, and the signal gain is independent of the offset. The disadvantage of this circuit is that the addition of R3 increases the noise gain, and hence the sensitivity to the op amp input offset voltage and noise. The input/output equation is given by:

$$V_{OUT} = -(R2/R1) \bullet V_{IN} - (R2/R3) \bullet V_{REF} \qquad \text{Eq. 6.2}$$

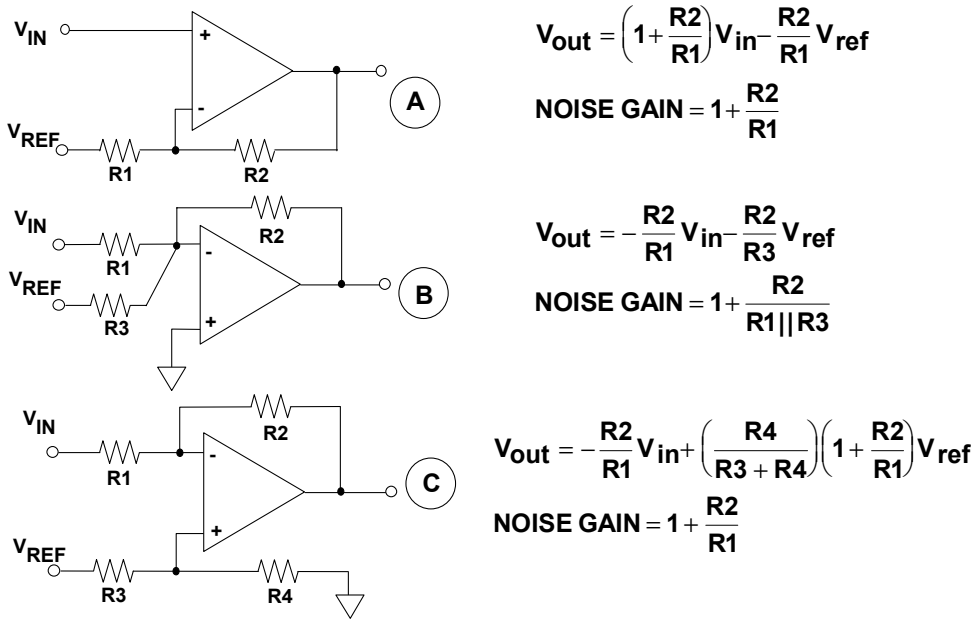



***Figure 6.10:*** *Op Amp Gain and Level Shifting Circuits*

The circuit in Figure 6.10C also operates in the inverting mode, and the offset voltage $V_{REF}$ is applied to the non-inverting input without noise gain penalty. This circuit is also attractive for single-supply applications ($V_{REF} > 0$). The input/output equation is given by:

$$V_{OUT} = -(R2/R1) \bullet V_{IN} + [R4/(R3+R4)][\ 1 + (R2/R1)] \bullet V_{REF} \qquad \text{Eq. 6.3}$$

Note that the circuit of Fig. 6.10A is sensitive to the impedance of $V_{REF}$, unlike the counterparts in B and C. This is due to the fact that the signal current flows into/from $V_{REF}$, due to $V_{IN}$ operating the op amp over its common-mode range. In the other two circuits the common-mode voltages are fixed, and no signal current flows in $V_{REF}$.

The circuit of Figure 6.10C is ideally suited to a single-supply level shifter and is identical to the one previously shown in Figure 6.5. It will now be examined further in light of single-supply and common-mode issues. Figure 6.11 shows this type of level shifter driving an ADC with an input range of +1.5 V to +3.5 V. Note that the circuit operates on a single +5-V supply.

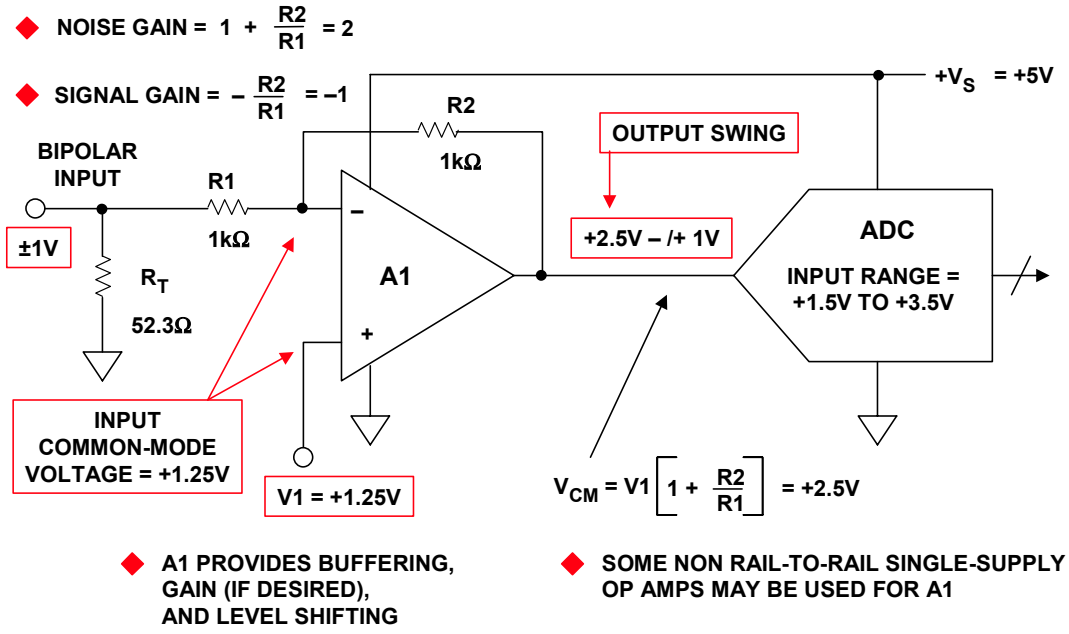



***Figure 6.11:*** *Single-Ended Single-Supply DC-Coupled Level Shifter*

The input range of the ADC (+1.5 V to +3.5 V) determines the output range of the A1 op amp. Since most complementary emitter follower output stages (see Figure 6.8C) will drive to within 1 V of either rail, a rail-to-rail output stage is not required.

The input common-mode voltage of A1 is set at +1.25 V which generates the required output offset of +2.5 V. Note that many non rail-to-rail single-supply op amps (such as the AD8057) can accommodate this input common-mode voltage when operating on a single +5-V supply. This circuit is an excellent example of where careful analysis of dc voltages is invaluable to the amplifier selection process. However, if we modify the circuit slightly as shown in Figure 6.12, an entirely different set of input/output requirements is placed on the op amp.

The input range of the ADC in Figure 6.12 is now +0.5 V to +2.5 V, and the entire circuit must operate on a +3-V power supply. A rail-to-rail output op amp is therefore required for A1 in order to ensure adequate output signal swing. Note that in addition, the input common-mode voltage of A1 is now +0.3 V in order to set the output common-mode voltage of +1.5 V (noise gain = +5, signal gain = –4). In order to allow an input common-mode voltage of +0.3 V, A1 must have either a PNP or PMOS input stage or a rail-to-rail input stage as previously shown in Figure 6.7.

This simple example serves to illustrate the importance of carefully examining the input/output signal level requirements placed on the op amp by the circuit conditions and the ADC interface. After the amplifier signal level requirements are established, then ac performance should be determined.

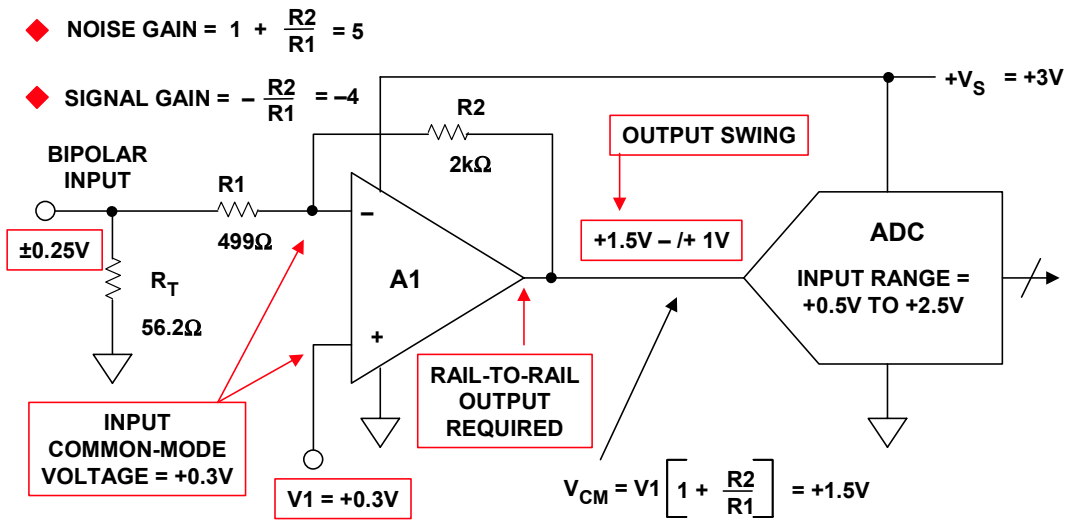



***Figure 6.12:*** *Single-Ended Level Shifter with Gain Requires Rail-to-Rail Op Amp*

### Op Amp AC Specifications and Data Converter Requirements

Modern op amps come with what may appear to be a relatively complete set of dc and ac specifications—however fully specifying an op amp under all possible circuit conditions is almost impossible. For example, Figure 6.13 shows some key specifications taken from the table of specifications on the datasheet for the AD8057/AD8058 high speed, low distortion op amp (Reference 2). Note that the specifications depend on the supply voltage, the signal level, output loading, etc. It should also be emphasized that it is customary to provide only *typical* ac specifications (as opposed to *maximum* and *minimum* values) for most op amps. In addition, we have seen that there are restrictions on the input and output common-mode signal ranges, which are especially important when operating on low voltage dual (or single) supplies.

| SPECIFICATION | $V_S$ = ±5V | $V_S$ = +5V |
|---|---|---|
| Input Common Mode Voltage Range | –4.0V to +4.0V | +0.9V to +3.4V |
| Output Common Mode Voltage Range | –4.0V to +4.0V | +0.9V to +4.1V |
| Input Voltage Noise | 7nV/√Hz | 7nV/√Hz |
| Small Signal Bandwidth | 325MHz | 300MHz |
| THD @ 5MHz, $V_O$ = 2V p-p, $R_L$ = 1kΩ | – 85dBc | – 75dBc |
| THD @ 20MHz, $V_O$ = 2V p-p, $R_L$ = 1kΩ | – 62dBc | – 54dBc |

***Figure 6.13:*** *AD8057/AD8058 Op Amp Key Specifications, G = +1*

Most op amp datasheets contain a section that provides supplemental performance data for various other conditions not explicitly specified in the primary specification tables. For instance, Figure 6.14 shows the AD8057/AD8058 distortion as a function of frequency for G = +1 and $V_S$ = ±5 V. Unless it is otherwise specified, the data represented by these curves should be considered typical (it is usually marked as such).

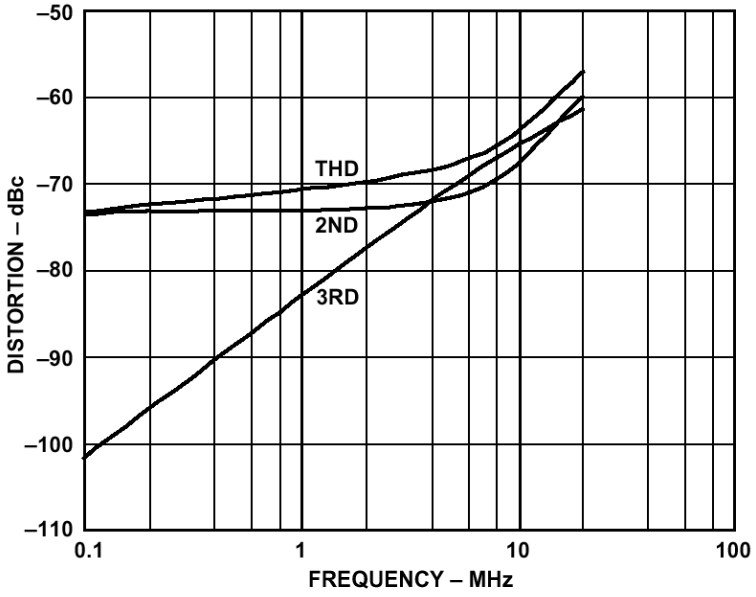



***Figure 6.14:*** *AD8057/AD8058 Op Amp Distortion Versus Frequency*
*G = +1, $R_L$ = 150 Ω, $V_S$ = ±5 V*

Note however that the data in both Figure 6.14 (and also the following Figure 6.15) is given for a dc load of 150 Ω. This is a load presented to the op amp in the popular application of driving a source and load-terminated 75-Ω cable. Distortion performance is generally better with lighter dc loads, such as 500 Ω to 1000 Ω (more typical of many ADC inputs), and this data may or may not be found on the datasheet.

On the other hand, Figure 6.15 shows distortion as a function of output signal level for a frequencies of 5 MHz and 20 MHz.

Whether or not specifications such as those just described are complete enough to select an op amp for an ADC driver application depends upon the ability to match op amp specifications to the actually required ADC operating conditions. In many cases, these comparisons will at least narrow the op amp selection process. The following sections will examine a number of specific driver circuit examples using various types of ADCs, ranging from high resolution measurement to high-speed, low distortion applications.

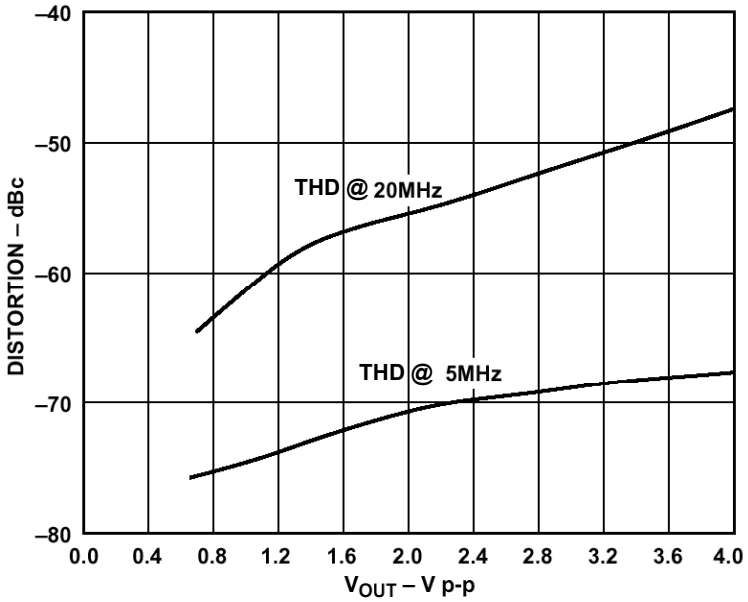



***Figure 6.15:*** *AD8057/AD8058 Op Amp Distortion Versus Output Voltage*
*G = +1, $R_L$ = 150 Ω, $V_S$ = ±5 V*

## Driving High Resolution Σ-Δ Measurement ADCs

The AD77xx family of ADCs is optimized for high resolution (16–24 bits) low frequency transducer measurement applications. Details of operation for this family can be found in Reference 3, and general characteristics of the family are listed in Figure 6.16.

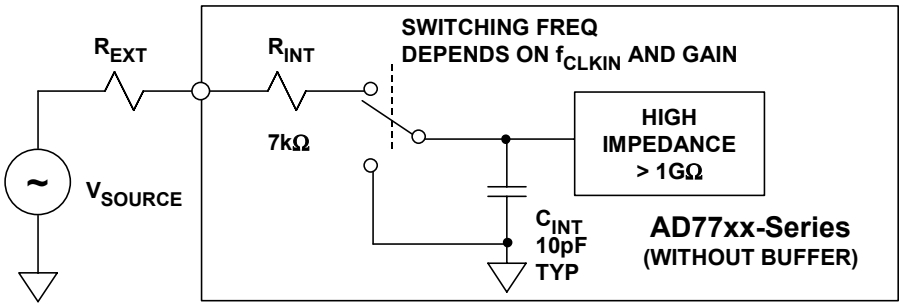
- **Resolution: 16 - 24 bits**
- **Input signal bandwidth: <60Hz**
- **Effective sampling rate: <100Hz**
- **Designed to interface directly to sensors (< 1 kΩ) such as bridges with no external buffer amplifier (e.g., AD77xx - series)**
  - **On-chip PGA and high resolution ADC eliminates the need for external amplifier**
- **If buffer is used, it should be precision low noise (especially 1/f noise)**
  - **OP1177**
  - **OP177**
  - **AD797**

***Figure 6.16:*** *Characteristics of AD77xx-family High Resolution Σ-Δ Measurement ADCs*

Some members of this family, such as the AD7730, have a high impedance input buffer which isolates the analog inputs from switching transients generated in the front-end programmable gain amplifier (PGA) and the Σ-Δ modulator. Therefore, no special

precautions are required in driving the analog inputs. Other members of the AD77xx family, however, either do not have the input buffer, or if one is included on-chip, it can be switched either in or out under program control. Bypassing the buffer offers a slight improvement in noise performance.

The equivalent input circuit of the AD77xx family without an input buffer is shown below in Figure 6.17. The input switch alternates between the 10-pF sampling capacitor and ground. The 7-kΩ internal resistance, $R_{INT}$, is the on-resistance of the input multiplexer. The switching frequency is dependent on the frequency of the input clock and also the internal PGA gain. If the converter is working to an accuracy of 20-bits, the 10-pF internal capacitor, $C_{INT}$, must charge to 20-bit accuracy during the time the switch connects the capacitor to the input. This interval is one-half the period of the switching signal (it has a 50% duty cycle). The input RC time constant due to the 7-kΩ resistor and the 10-pF sampling capacitor is 70 ns. If the charge is to achieve 20-bit accuracy, the capacitor must charge for at least 14 time constants, or 980 ns. Any external resistance in series with the input will increase this time constant.




- **$R_{EXT}$ Increases $C_{INT}$ Charge Time and May Result in Gain Error**
- **Charge Time Dependent on the Input Sampling Rate and Internal PGA Gain Setting**
- **Refer to Specific Data Sheet for Allowable Values of $R_{EXT}$ to Maintain Desired Accuracy**
- **Some AD77xx-Series ADCs Have Internal Buffering Which Isolates Input from Switching Circuits**

***Figure 6.17:*** *Driving Unbuffered AD77xx-Series Σ-Δ ADC Inputs*

There are tables on the datasheets for the various AD77xx ADCs, which give the maximum allowable values of $R_{EXT}$ in order to maintain a given level of accuracy. These tables should be consulted if the external source resistance is more than a few kΩ.

Note that for instances where an external op amp buffer is found to be required with this type of converter, guidelines exist for best overall performance. This amplifier should be a precision low-noise bipolar-input type, such as the OP1177, OP177, or the AD797.

## Driving Single-Ended Input Single-Supply 1.6-V to 3.6-V Successive Approximation ADCs

The need for low power, low supply voltage ADCs in small packages led to the development of the AD7466/AD7467/AD7468 12-/10-/ and 8-bit family of converters (Reference 4). These devices operate on supply voltages from 1.6 V to 3.6 V and utilize a successive approximation architecture which allows sampling rates up to 200 kSPS. The converters are packaged in a 6-lead SOT-23 package and offer this performance at only 0.62 mW with a 3-V supply and 0.12 mW with a 1.6-V supply. An automatic power-down mode reduces the supply current to 8 nA. Data is transferred via a simple serial interface. It is useful to examine these converters in more detail, because they illustrate some of the tradeoffs which must be made in designing appropriate interface circuits.

A simplified block diagram of the series is shown in Figure 6.18. As mentioned, the ADC utilizes a standard successive approximation architecture based on a switched capacitor CMOS charge redistribution DAC. The input CMOS switches, SW1 and SW2, comprise the sample-and-hold function, and are shown in the track mode in the diagram. Capacitor C1 represents the equivalent parasitic input capacitance, $C_H$ is the hold capacitor, and $R_S$ is the equivalent on-resistance of SW2. In the track mode, SW1 is connected to the input, and SW2 is closed. In this condition, the comparator is balanced, and the hold capacitor $C_H$ is charged to the value of the input signal. Assertion of the $\overline{CS}$ (convert start) starts the conversion process: SW2 opens, and SW1 is connected to ground, causing the comparator to become unbalanced. The control logic and the charge redistribution DAC are used to add and subtract fixed amounts of charge from the hold capacitor to bring the comparator back into balance. At the end of the appropriate number of clock pulses, the conversion is complete.

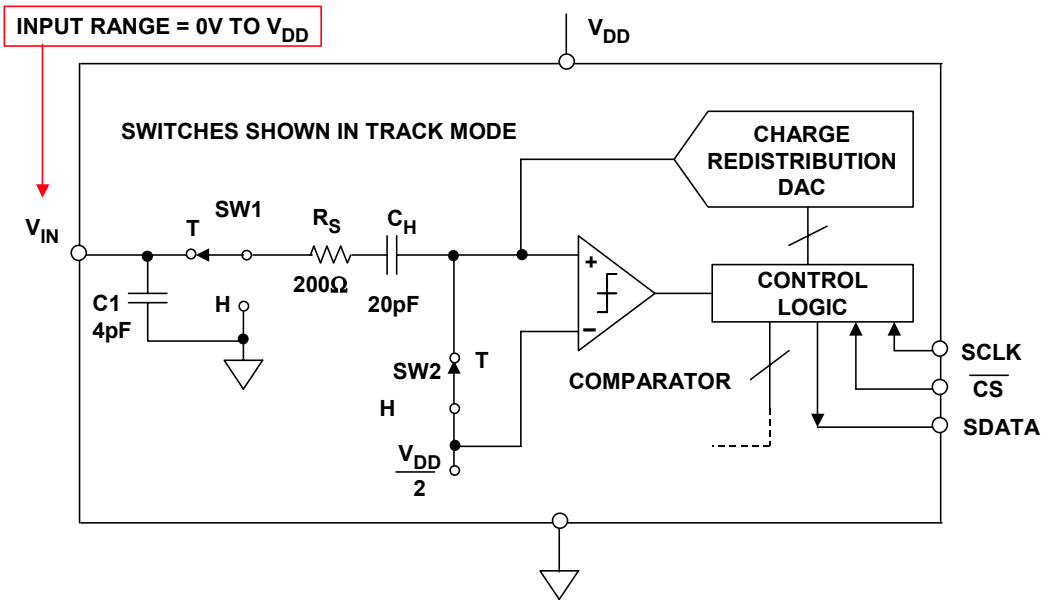



***Figure 6.18:*** *Input Circuit of AD7466 1.6-V to 3.6-V, 12-Bit, 200-kSPS SOT-23-6 ADC*

The switching action of CMOS switches SW1 and SW2 places certain requirements on the input drive circuit with respect to the transient currents. In addition, the input signal must charge and discharge $C_H$ in the track mode. In most cases, no input drive amplifier is required provided the source impedance is less than 1 kΩ (although a slight degradation in THD will be observed at input frequencies approaching 100 kHz).

The input voltage range of the AD746x ADC is from 0 V to the supply voltage, and the supply also acts as the reference. If more accuracy or stability is required, the supply voltage can be derived from a voltage reference or an LDO.

Although single-supply rail-to-rail 1.8-V op amps are available (such as the AD8515, AD8517, and AD8631), these op amps will not drive signals completely to either rail due to the saturation voltage of the output transistors (this has previously been discussed in detail). If these are used as drive amplifiers to the AD746x, the usable input range of the ADC will be reduced by an amount which depends not only on this saturation voltage but the amount of additional headroom required at the amplifier output in order to give acceptable distortion performance at the higher input frequencies.

The overall conclusion of this discussion is that low voltage single-supply ADCs such as the AD746x are best driven directly from low impedance sources (< 1 kΩ). If a drive amplifier is required, it must operate on a higher supply voltage in order to utilize the full input range of the ADC.

## Driving Single-Supply ADCs with Scaled Inputs

Even with the widespread popularity of single-supply systems, there are still applications where it is desirable for the ADC to process bipolar input signals. This can be handled in a number of ways, but a simple method is to provide an appropriate thin-film resistive divider/level-shifter at the input of the ADC. The AD789x and AD76xx family of single supply SAR ADCs (as well as the AD974, AD976, and AD977) include such a thin film resistive attenuator and level shifter on the analog input to allow a variety of input range options, both bipolar and unipolar.

A simplified diagram of the input circuit of the AD7890-10 12-bit, 8-channel ADC is shown in Figure 6.19 (Reference 5). This arrangement allows the converter to digitize a ±10-V input while operating on a single +5-V supply.

Within the ADC, the R1/R2/R3 thin film network provides attenuation and level shifting to convert the ±10-V input to a 0-V to +2.5-V signal that is digitized. This type of input requires no special drive circuitry, because R1 isolates the input from the actual converter circuitry that may generate transient currents due to the conversion process. Nevertheless, the external source resistance $R_S$ should be kept reasonably low, to prevent gain errors caused by the $R_S$/R1 divider.

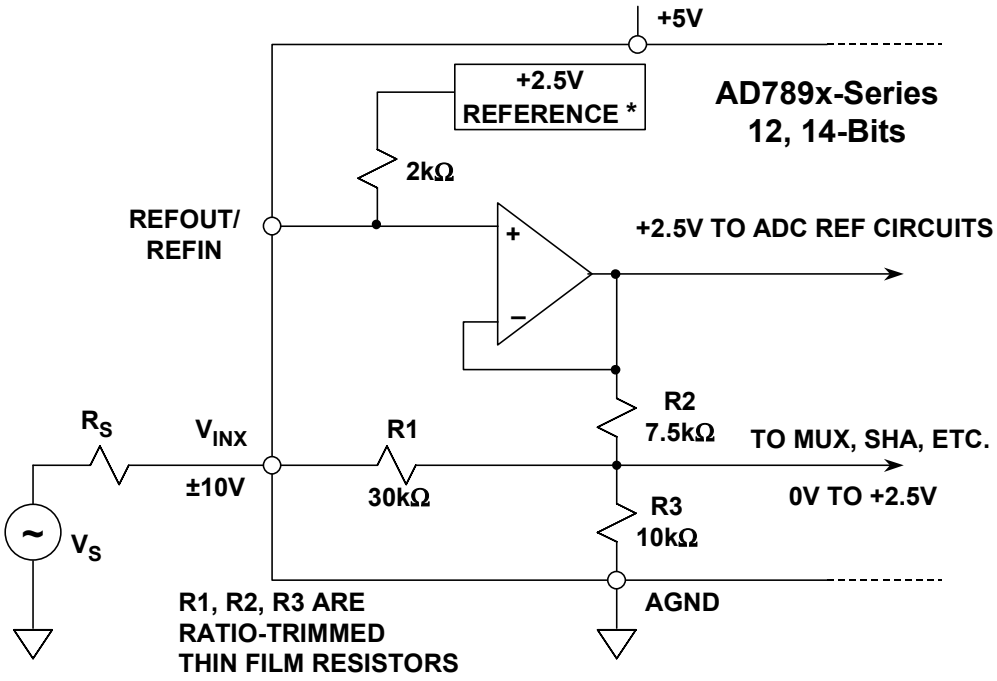
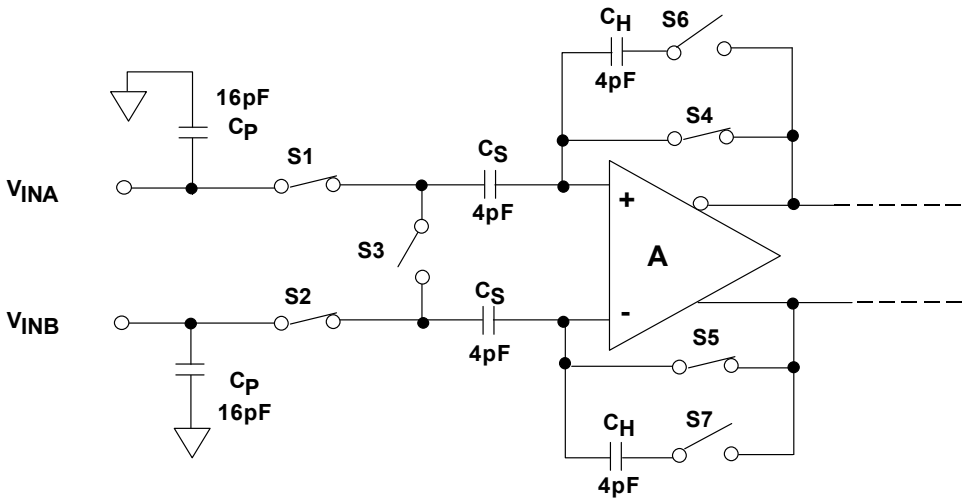



***Figure 6.19:*** *Driving Single-Supply Data Acquisition ADCs With Scaled Inputs*

## Driving Differential Input CMOS Switched Capacitor ADCs

CMOS ADCs are quite popular because of their low power, high performance, and low cost. The equivalent input circuit of a typical CMOS ADC using a differential sample-and-hold is shown in Figure 6.20. While the switches are shown in the *track* mode, note that they open/close at the sampling frequency. The 16-pF capacitors represent the effective capacitance of switches S1 and S2, plus the stray input capacitance. The $C_S$ capacitors (4 pF) are the sampling capacitors, and the $C_H$ capacitors are the hold capacitors. Although the input circuit is completely differential, this ADC structure can be driven either single-ended or differentially. Optimum performance, however, is generally obtained using a differential transformer or differential op amp drive.

In the *track* mode, the differential input voltage is applied to the $C_S$ capacitors. When the circuit enters the *hold* mode, the voltage across the sampling capacitors is transferred to the $C_H$ hold capacitors and buffered by the amplifier A (the switches are controlled by the appropriate sampling clock phases). When the SHA returns to the *track* mode, the input source must charge or discharge the voltage stored on $C_S$ to the new input voltage. This action of charging and discharging $C_S$, averaged over a period of time and for a given $f_S$ sampling frequency, makes the input impedance appear to have a benign resistive component. However, if this action is analyzed within a sampling period ($1/f_S$), the input impedance is dynamic, and certain input drive source precautions should be observed.




**SWITCHES SHOWN IN TRACK MODE**

***Figure 6.20:*** *Simplified Input Circuit for a Typical Switched Capacitor CMOS Sample-and-Hold*

The resistive component of the input impedance can be computed by calculating the average charge that is drawn by $C_H$ from the input drive source. It can be shown that if $C_S$ is allowed to fully charge to the input voltage before switches S1 and S2 are opened that the average current into the input is the same as if there were a resistor equal to $1/(C_S f_S)$ connected between the inputs. Since $C_S$ is only a few picofarads, this resistive component is typically greater than several kΩ for an $f_S$ = 10 MSPS.

Over a sampling period, the SHA's input impedance appears as a dynamic load. When the SHA returns to the track mode, the input source should ideally provide the charging current through the $R_{ON}$ of switches S1 and S2 in an exponential manner. The requirement of exponential charging means that the source impedance should be both low and resistive up to and beyond the sampling frequency.

A differential input CMOS ADC can be driven single-ended with some ac performance degradation. An important consideration in CMOS ADC applications are the input switching transients previously discussed. Typical single-ended transients for a CMOS ADC are shown in Figure 6.21 for the AD9225 12-bit, 25-MSPS ADC. This data was taken driving the ADC with an equivalent 50-Ω source impedance. During the sample-to-hold transition, the input signal is sampled when $C_S$ is disconnected from the source. Notice that during the hold-to-sample transition, $C_S$ is reconnected to the source for recharging. The transients consist of linear, nonlinear, and common-mode components at the sample rate.

- **Hold-to-Sample Mode Transition- $C_S$ Returned to Source for "recharging". Transient Consists of Linear, Nonlinear, and Common-Mode Components at Sample Rate .**
- **Sample-to-Hold Mode Transition- Input Signal Sampled when $C_S$ is disconnected from Source.**

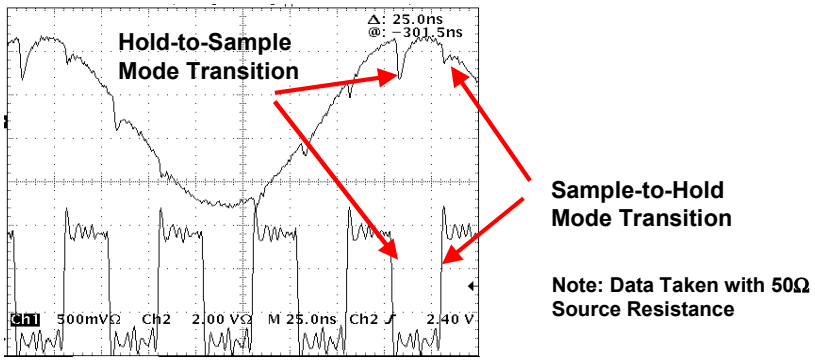



***Figure 6.21:*** *Single-Ended Input Transients for a Typical CMOS ADC Sampling at 25 MSPS*

### Single-Ended Drive Circuits for Differential Input CMOS ADCs

A few simple single-ended drive circuits suitable for CMOS ADCs will now be examined. Although differential drive is preferable for best ac performance, single-ended drivers are often adequate in less demanding applications.

Figure 6.22 shows a generalized single-ended op amp driver for a CMOS ADC. In this circuit, series resistor $R_S$ has a dual purpose. Typically chosen in the range of 25-100 Ω, it limits the peak transient current from the driving op amp. Importantly, it also decouples the driver from the ADC input capacitance (and possible phase margin loss).

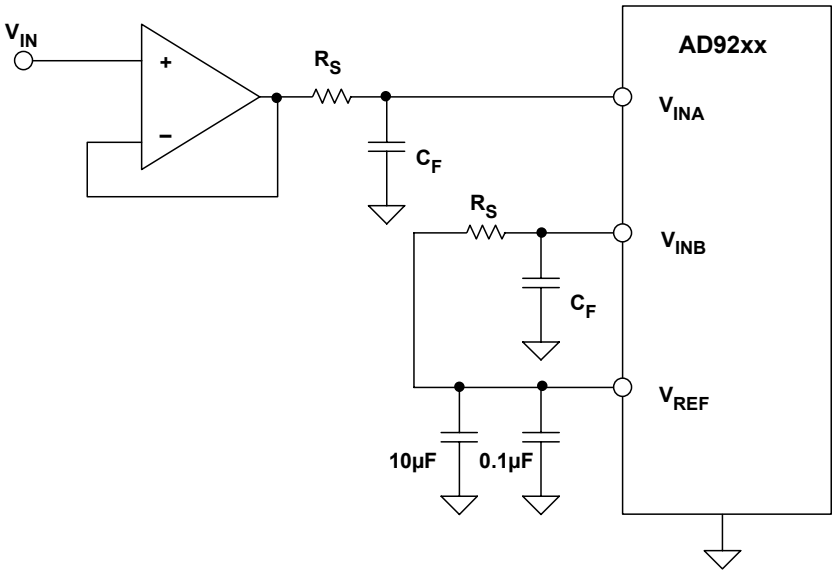



***Figure 6.22:*** *Optimizing a Single-Ended Switched Capacitor ADC Input Drive Circuit*

Another feature of the circuit are the dual networks of $R_S$ and $C_F$. Matching both the dc and ac source impedance for the ADC's $V_{INA}$ and $V_{INB}$ inputs ensures symmetrical settling of common-mode transients, for optimum noise and distortion performance. At both inputs, the $C_F$ shunt capacitor also acts as a charge reservoir and steers the common-mode transients to ground.

In addition to the buffering of transients, $R_S$ and $C_F$ also form a lowpass filter for $V_{IN}$, which limits the output noise of the drive amplifier into the ADC input $V_{INA}$. The exact values for $R_S$ and $C_F$ are generally optimized within the circuit, and the recommended values given on the ADC datasheet.

Many important factors should be considered in selecting an appropriate drive amplifier. As discussed previously, common-mode input and output voltages must be compatible with the ADC power supply and input range. The op amp noise and distortion performance should be compatible with the expected performance of the ADC. In addition, the settling time of the op amp should be fast enough so that the output can settle from the transient currents produced by the ADC. A good guideline is that the 0.1% settling time of the op amp should be no more than one-half the period of the maximum sampling frequency. The most important factor is simply to consult the ADC data sheet for recommended drive op amps and the associated circuits.

A generalized dc-coupled single-ended op amp driver and level shifter for the AD922x-series of ADCs is shown in Figure 6.23. The values in this circuit are suitable for sampling rates up to about 25 MSPS. This circuit interfaces a ±2-V ground-referenced input signal to the single-supply ADC, and also provides transient current isolation. The ADC input voltage range is 0 to +4-V, and a dual supply op amp is required, since the ADC minimum input is 0 V.

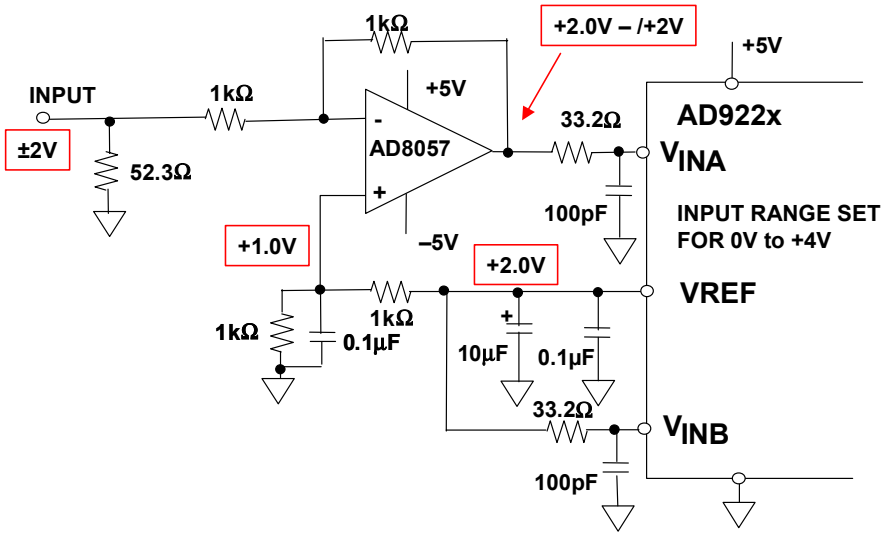



***Figure 6.23:*** *Single-Ended DC-Coupled Level Shifter and Driver for the AD922x ADC*

The non-inverting input of the AD8057 is biased at +1 V, which sets the output common-mode voltage at $V_{INA}$ to +2 V for a bipolar input signal source. Note that the $V_{INA}$ and $V_{INB}$ source impedances are matched for better common-mode transient cancellation. The 100-pF capacitors act as small charge reservoirs for the input transient currents, and also form lowpass noise filters with the 33.2-Ω series resistors.

A similar single-ended level shifter and driver is shown in Figure 6.24, however this circuit is designed to operate on a single +5-V supply. In this circuit the bipolar ±1-V input signal is interfaced to the input of the ADC whose range is set for 2 V about a +2.5-V common-mode voltage. The AD8061 rail-to-rail output op amp is used, although others are suitable depending upon bandwidth and distortion requirements (for example, the AD8027, AD8031, or AD8091). The +1.25-V input common-mode voltage for the AD8061 is developed by a voltage divider from the external AD780 2.5-V reference.

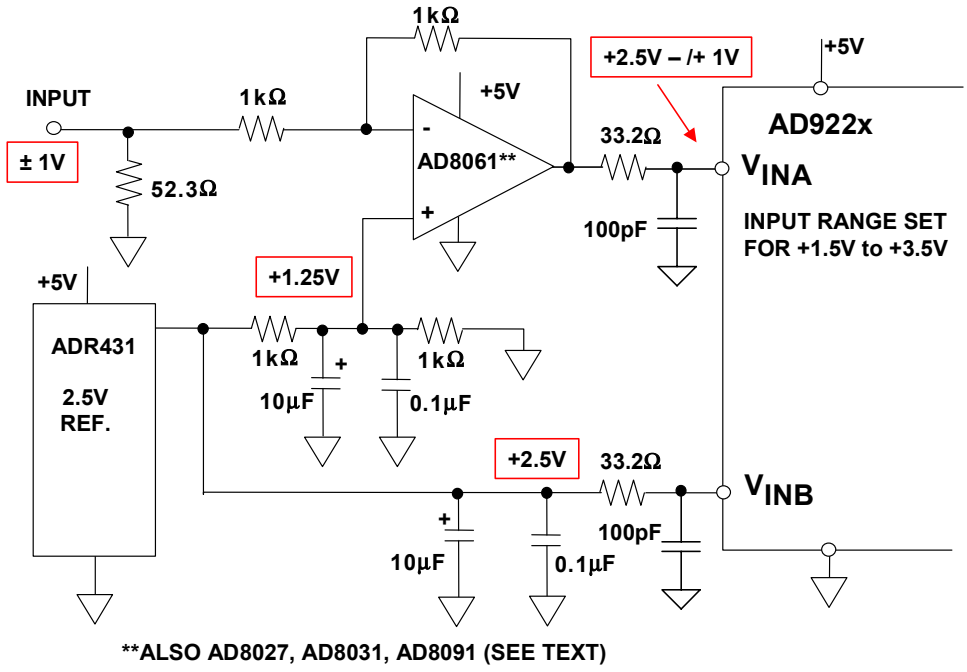



***Figure 6.24:*** *Single-Ended DC-Coupled Single-Supply Level Shifter for Driving AD922x ADC*

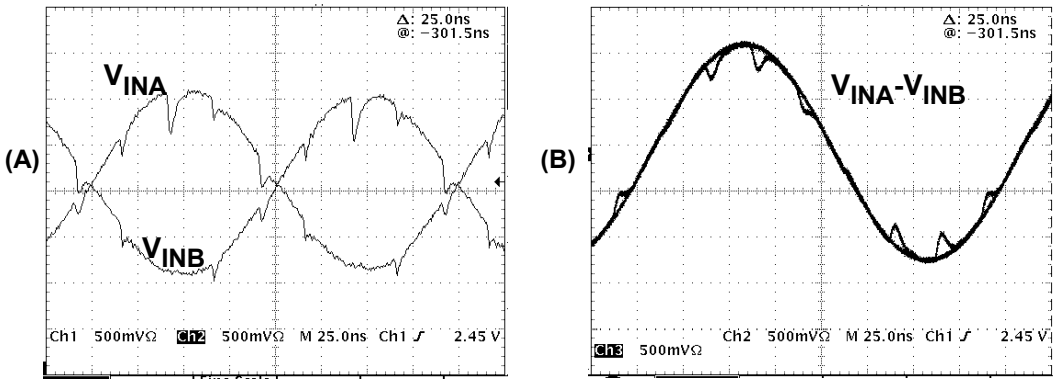
## Differential Input ADC Drivers

As previously discussed, most high performance ADCs are now being designed with differential inputs. A fully differential ADC design offers the advantages of good common-mode rejection, reduction in second-order distortion products, and simplified factory trimming algorithms. Although most differential input ADCs can be driven single-ended as previously described, a fully differential driver usually optimizes overall performance.

In the following discussions, it is useful to keep in mind that there are currently two popular IC processes used for high performance ADCs, and each one has certain application implications. Many medium-to-high performance ADCs are fabricated on high density foundry CMOS processes, and these typically use switched capacitor

sample-and-hold techniques (previously described) which tend to generate transient currents at the ADC inputs. In many cases, however, ultra high performance ADCs are designed on either BiCMOS (bipolar and CMOS devices on the same process) or CB (complementary bipolar) processes. ADCs designed on BiCMOS or CB processes typically provide input buffers as part of a more conventional diode-switched sample-and-hold circuit which minimize the effects of input transient currents—however, the input range is generally less flexible than in CMOS-based designs.

In order to understand the advantages of common-mode rejection of input transient currents, we will next examine the waveforms at the two inputs of the AD9225 12-bit, 25-MSPS CMOS ADC as shown in Figure 6.25A, designated as $V_{INA}$ and $V_{INB}$. The balanced source impedance is 50 Ω, and the sampling frequency is set for 25 MSPS. The diagram clearly shows the switching transients due to the internal ADC switched capacitor sample-and-hold. Figure 6-25B shows the difference between the two waveforms, $V_{INA} - V_{INB}$.




- **Differential charge transient is symmetrical around mid-scale and dominated by linear component**
- **Common-mode transients cancel with equal source impedance**

**Note: Data Taken with 50Ω Source Resistances**

***Figure 6.25:*** *Typical Single-Ended (A) and Differential (B) Input Transients of CMOS Switched Capacitor ADC Sampling at 25 MSPS*

Note that the resulting differential charge transients are symmetrical about mid-scale, and that there is a distinct linear component to them. This shows the reduction in the common-mode transients, and also leads to better distortion performance than would be achievable with a single-ended input.

Transformer coupling into a differential input ADC provides excellent common-mode rejection and low distortion, provided performance to dc is not required. Figure 6.26 shows a typical circuit. The transformer is a Mini-Circuits RF transformer, model #ADT4-1WT which has an impedance ratio of 4 (turns ratio of 2). The 3-dB bandwidth of this transformer is 2 MHz to 775 MHz (Reference 6). The schematic assumes that the signal source impedance is 50 Ω. The 1:4 impedance ratio requires the 200-Ω secondary termination for optimum power transfer and low VSWR. The center tap of the

transformer secondary winding provides a convenient means of level shifting the input signal to the optimum $V_C/2$ common-mode voltage of the ADC (some ADCs may have a common-mode voltage different than $V_C/2$, so the data sheet should be consulted).

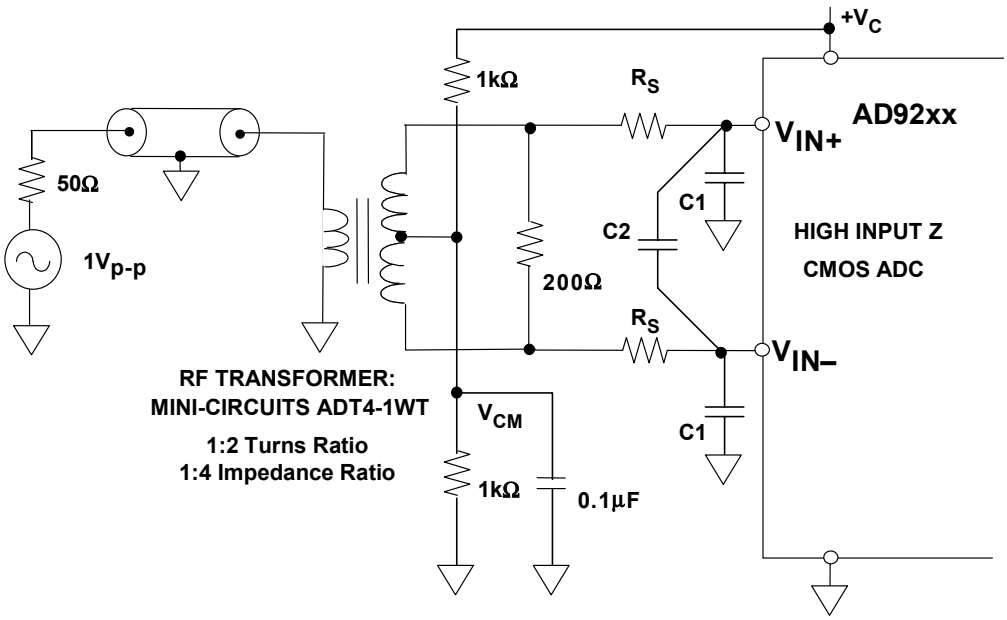
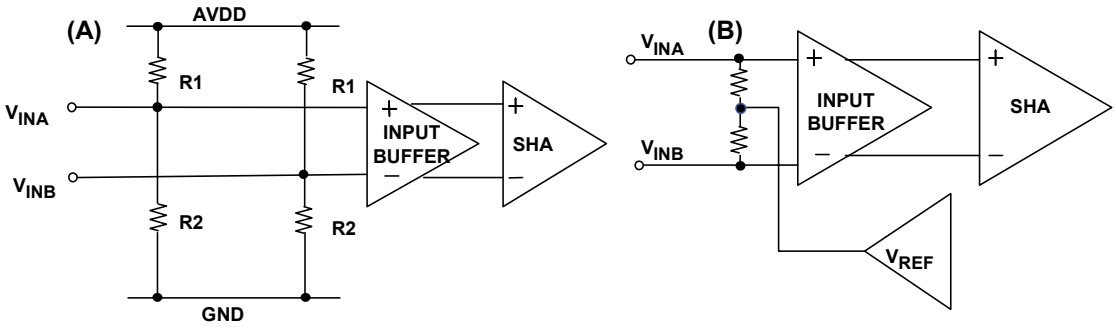



***Figure 6.26:*** *Transformer Coupling into a Differential Input CMOS ADC*

Transformers with other turns ratios may also be selected to optimize the performance for a given application. For example, a given input signal source or amplifier may realize an improvement in distortion performance at reduced output power levels and signal swings. Hence, selecting a transformer with a higher impedance ratio effectively "steps up" the signal level thus reducing the driving requirements of the signal source.

The network consisting of $R_S$, C1, and C2 is relatively common when driving CMOS switched capacitor ADC inputs with a transformer. The $R_S$ resistors serve to isolate the transformer secondary winding from the switching transients, and the optimum value (determined empirically) generally ranges from 25 to 100 Ω. The C1 capacitors serve as common-mode charge reservoirs for the switching transients and also provide noise filtering (in conjunction with the $R_S$ resistors). The C1 capacitors should have no greater than 5% tolerance to prevent common-mode to differential signal conversion. If needed, C2 can be added for additional differential filtering. Data sheets for most CMOS ADCs typically recommend optimum values for $R_S$, C1, and C2 and should be consulted in all cases.

As previously mentioned, BiCMOS or complementary bipolar ADCs typically provide some amount of input buffering, and therefore have lower input transient currents than CMOS converters. Figure 6.27 shows two typical input configurations for buffered BiCMOS or CB ADCs. Although this can simplify the interface, the fixed input common-mode level may limit flexibility. In Figure 6.27A the common-mode voltage is developed with a resistive divider connected between ground and the positive analog supply voltage. In Figure 6.27B, the common-mode voltage is generated by an internal reference voltage.




- **Input buffers typical on BiCMOS and bipolar processes**
- **Difficult on CMOS**
- **Simplified input interface - low transient currents**
- **Fixed common-mode level may limit flexibility**

***Figure 6.27:*** *ADCs with Buffered Differential Inputs (BiCMOS or Complementary Bipolar Process)*

Figure 6.28 shows a transformer drive circuit for the AD9430 12-bit, 170-/210-MSPS BiCMOS ADC (Reference 7). For best performance at high input frequencies, two transformers are connected in series as shown to minimize even-order harmonic distortion. The first transformer converts the single-ended signal to a differential signal—however the grounded input on the primary side degrades the amplitude balance on the secondary winding because of the stray capacitive coupling between the windings. The second transformer improves the amplitude balance, and thus the harmonic distortion. A wideband transformer, such as the Mini Circuits ADT1-1WT is recommended for these applications. The 3-dB bandwidth of the ADT1-1WT is 0.4 MHz to 800 MHz. Note that the bandwidth through the two transformers is equal to the bandwidth of a single transformer divided by √2.

The net impedance seen by the secondary winding of the second transformer is the sum of the ADC input impedance (6 kΩ) and the two 24.9-Ω series resistors, or approximately 6050 Ω. The 51.1-Ω termination resistor in parallel with 6050 Ω yields the desired impedance of approximately 50 Ω.

There is no requirement for input filtering, since the BiCMOS buffered input circuit generates minimal transient currents. The 24.9-Ω series resistors simply buffers the transformer from the small input capacitance of the ADC (~5 pF). The input common-mode voltage is set at +2.8 V by the 3.5-kΩ/20-kΩ resistive divider (when operating on a +3.3-V supply). This serves to illustrate the point made earlier that BiCMOS and complementary bipolar ADCs may not have a common-mode voltage that is exactly mid-supply. In this circuit, the most positive input voltage on either input is 2.8 V + 0.384 V = 3.184 V which is only 116 mV from the +3.3-V supply. The implication therefore is that for low distortion performance in a 3.3-V system, the AD9430 must either be driven from a transformer or from an ac-coupled differential amplifier.

If dc coupling is required, the driving amplifier must operate on a higher supply voltage, because even rail-to-rail output stages will give poor high frequency distortion performance if only 116-mV of headroom is available.

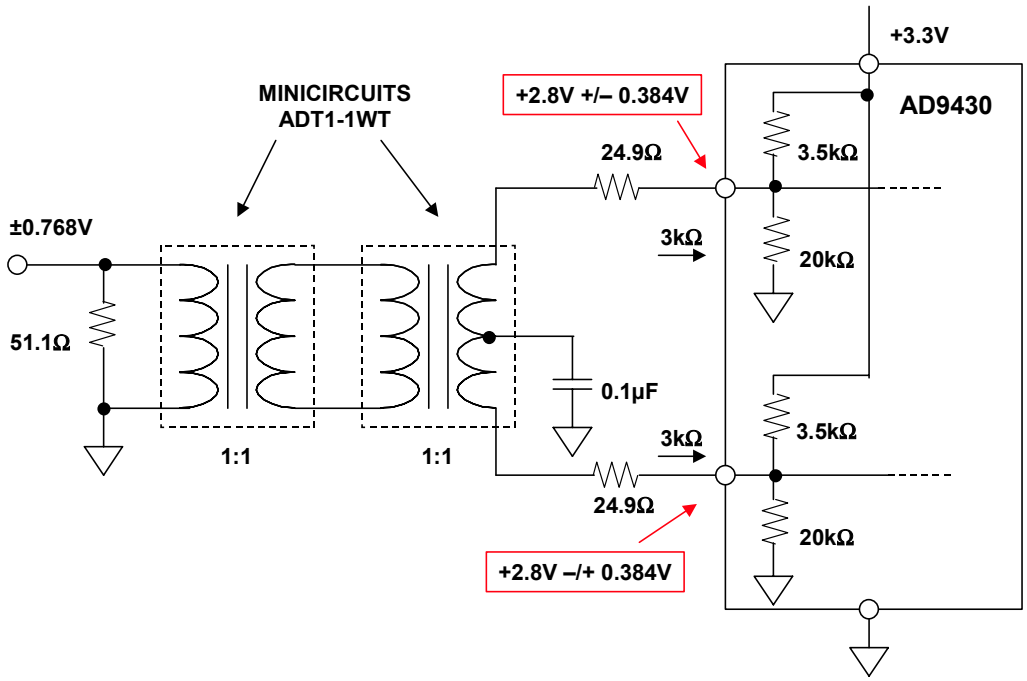



***Figure 6.28:*** *Transformer Coupling into the AD9430 12-Bit, 170-/210-MSPS BiCMOS ADC*

Note that the center tap of the secondary winding of the transformer is decoupled to ground to ensure a balanced drive.

A similar transformer drive circuit for the AD6645 14-bit, 80-/105-MSPS (bipolar process) ADC is shown in Figure 6.29 (Reference 8). Note that the input common-mode voltage is developed by the two 500-Ω resistors connected to each input from the internal 2.4-V reference. The differential input resistance of the ADC is therefore 1 kΩ. As in the previous circuit, the 24.9-Ω series resistors isolate the transformer secondary winding from the small input capacitance of the ADC. The net differential impedance seen by the secondary winding of the transformer is therefore 1050 Ω.

In this circuit, a Mini Circuits ADT4-1WT 1:4 impedance ratio (1:2 turns ratio) transformer is used to match the 1050-Ω differential resistance to the 50-Ω source. The 1050-Ω resistance is 262.5 Ω referred to the primary winding, and the 61.9-Ω termination resistor in parallel with 262.5 Ω is approximately 50 Ω. The 3-dB bandwidth of the transformer is 2 MHz to 775 MHz.

Theoretically, a 1:20 impedance ratio (corresponding to a 1 : 4.47 turns ratio) transformer would perfectly match the AD6645 1000-Ω input to the 50-Ω source and provide a "noise-free" voltage gain of 4.47 (+13 dB). However, this large turns ratio could result in unsatisfactory bandwidth and distortion performance.

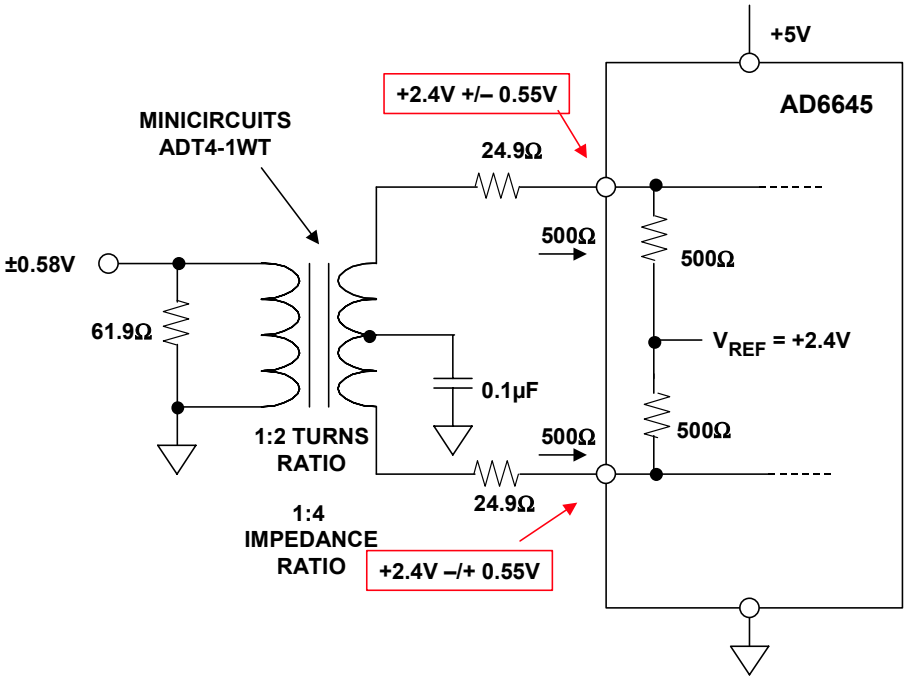



***Figure 6.29:*** *Transformer Coupling into the AD6645 14-Bit, 80-/105-MSPS Complementary Bipolar Process ADC*

To illustrate the effects of utilizing transformers for voltage gain on system noise figure (NF), Figure 6.30 shows the AD6645 sampling a 40-MHz bandwidth signal at 80 MSPS for turns ratios of 1:1 (Figure 6.30A), 1:2 (Figure 6.30B) and 1:4 (Figure 6.30C). (Refer back to Chapter 2 for the basic definitions and calculations of ADC noise figure).

Notice that each time the turns ratio is doubled, the noise figure decreases by 6 dB. In practice, however, empirical data indicates that bandwidth and distortion are compromised when driving the AD6645 with a turns ratio of greater than 1:2.

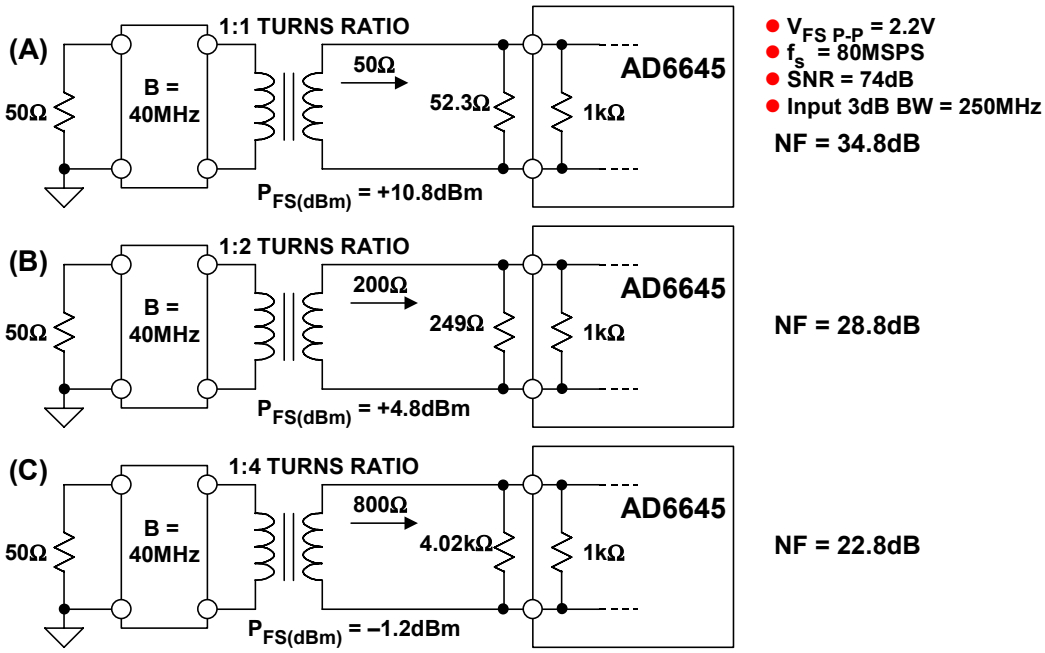



***Figure 6.30:*** *Using RF Transformers to Improve Overall ADC Noise Figure*

## Driving ADCs with Differential Amplifiers

Certainly for most RF and IF applications, transformer ADC drivers yield the best overall distortion and noise performance, especially if the transformer can be utilized to achieve some amount of "noise free" voltage gain. There are, however, many applications where differential input ADCs cannot be driven with transformers because the frequency response must extend to dc. In these cases, the op amp common-mode input and output voltage, gain, distortion, and noise must be carefully considered in designing dc-coupled drive circuitry. The following two subsections discuss two types of differential op amp drivers: the first is based on utilizing dual op amps, and the second utilizes fully integrated differential amplifiers.

### Dual Op Amp Drivers

Figure 6.31 shows how the dual AD8058 op amp can be connected to convert a single-ended bipolar signal to a differential one suitable for driving the AD92xx family of CMOS ADCs. Utilizing a dual op amp provides better gain and phase matching than would be achieved by simply using two single op amps. The input range of the ADC is set for a 2-V p-p differential input signal (1-V p-p on each input), and a common-mode voltage of +2 V. As shown for previous CMOS ADCs, the 100-pF capacitors serve as charge reservoirs for the transient currents, and also act as lowpass noise filters in conjunction with the 33.2-Ω resistors.

The A1 amplifier is configured as a non-inverting op amp. The 1-kΩ divider resistors level shift the ±0.5-V input signal to +1 V ±0.25 V at the non-inverting input of A1. The output of A1 is therefore +2 V +/–0.5 V, because the non-inverting gain of A1 is 2.

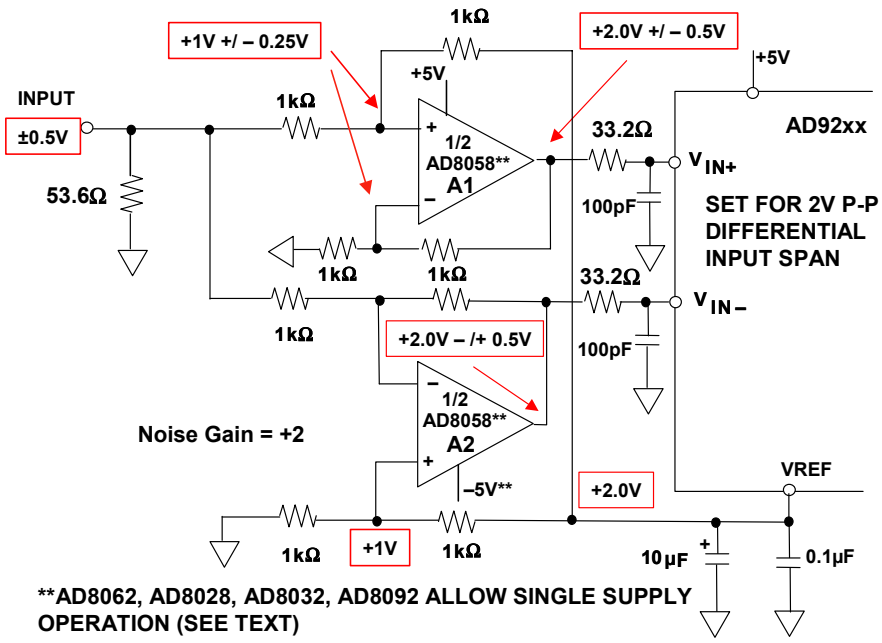



***Figure 6.31:*** *Op Amp Single-Ended to Differential DC-Coupled Driver with Level Shifting*

The A2 op amp inverts the input signal, and the 1-kΩ divider resistors establish a +1-V common-mode voltage on its non-inverting input. The output of A2 is therefore +2 V –/+0.5 V.

This circuit provides good matching between the two op amps because they are duals on the same die and are both operated at the same noise gain of 2. However, the input voltage noise of the AD8058 is 20 nV/√Hz, and this appears as 40 nV/√Hz at the output of both A1 and A2 thereby, introducing possible SNR degradation in some applications. In the circuit of Figure 6.31, this is mitigated somewhat by the input RC network which not only reduces the input noise, but also absorbs some of the transient currents.

The AD8058 op amp does not have rail-to-rail inputs or outputs, and the following simple analysis shows that the circuit as shown in Figure 6.31 must use dual supplies. The output common-mode voltage of the AD8058 operating on a single +5-V supply is +0.9 V to +3.4 V, which would be acceptable in this circuit, because the required signal swing is only +1.5 V to +2.5 V. However, the input common-mode voltage of the AD8058 operating on a single +5-V supply is specified as +0.9 V to +4.1 V; but the circuit requires that the input common-mode voltage go to +0.75 V, which is outside the allowable range. Therefore, a dual supply is required for the op amp.

If single supply operation is required, however, there are a number of dual rail-to-rail op amps which should be considered, such as the AD8062, AD8028, AD8032, and the AD8092.

**Fully Integrated Differential Amplifier Drivers**

A block diagram of the AD813x family of fully differential amplifiers optimized for ADC driving is shown in Figure 6.32 (see Reference 9). Figure 6.32A shows the details of the internal circuit, and Figure 6.32B shows the equivalent circuit. The gain is set by the external resistors $R_F$ and $R_G$, and the common-mode voltage is set by the voltage on the $V_{OCM}$ pin. The internal common-mode feedback forces the $V_{OUT+}$ and $V_{OUT-}$ outputs to be balanced, i.e., the signals at the two outputs are always equal in amplitude but 180° out of phase per the equation,

$$V_{OCM} = ( V_{OUT+} + V_{OUT-} ) / 2. \qquad \text{Eq. 6.4}$$

The AD813x uses two feedback loops to separately control the differential and common-mode output voltages. The differential feedback, set with external resistors, controls only the differential output voltage. The common-mode feedback controls only the common-mode output voltage. This architecture makes it easy to arbitrarily set the output common-mode level in level shifting applications. It is forced, by internal common-mode feedback, to be equal to the voltage applied to the $V_{OCM}$ input, without affecting the differential output voltage. The result is nearly perfectly balanced differential outputs of identical amplitude and exactly 180° apart in phase over a wide frequency range. The circuit can be used with either a differential or a single-ended input, and the voltage gain is equal to the ratio of $R_F$ to $R_G$.

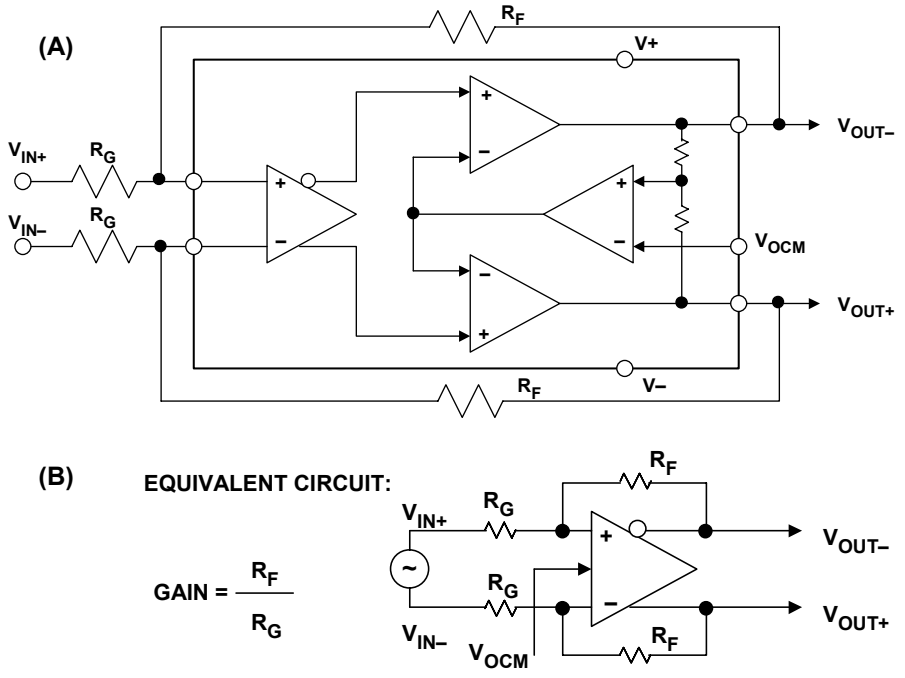
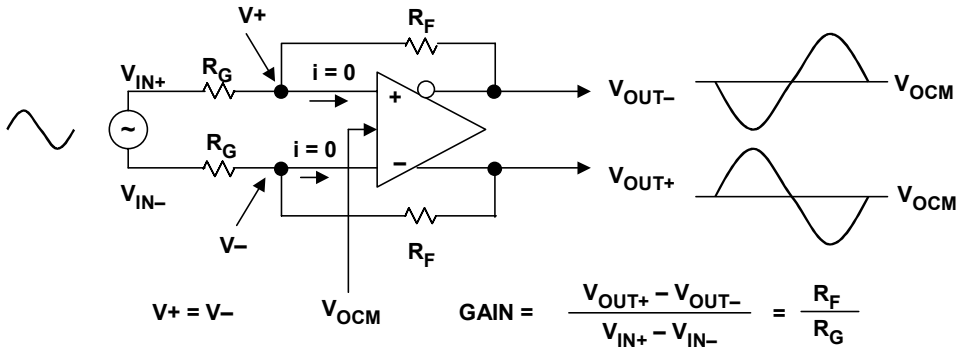



***Figure 6.32:*** *AD813x Differential ADC Driver Functional Diagram and Equivalent Circuit*

The circuit can be analyzed using the assumptions and procedures summarized in Figure 6.33. As in the case of op amp circuit dc analysis, one can first make the assumption that the currents into the inverting and non-inverting input are zero (i.e., the input impedances are high relative to the values of the feedback resistors). The second assumption is that feedback forces the non-inverting and inverting input voltages to be equal. The third assumption is that the output voltages are 180° out of phase and symmetrical about $V_{OCM}$.




- + and – input currents are zero
- + and – input voltages are equal
- Output voltages are 180° out of phase and symmetrical about $V_{OCM}$
- Gain = $R_F/R_G$

***Figure 6.33:*** *Analyzing Voltage Levels in Differential Amplifiers*

Even if the external feedback networks ($R_F/R_G$) are mismatched, the internal common-mode feedback loop will still force the outputs to remain balanced. The amplitudes of the signals at each output will remain equal and 180° out of phase. The input-to-output differential-mode gain will vary proportionately to the feedback mismatch, but the output balance will be unaffected. Ratio matching errors in the external resistors will result in a degradation of the circuit's ability to reject input common-mode signals, much the same as for a four-resistor difference amplifier made from a conventional op amp.

Also, if the dc levels of the input and output common-mode voltages are different, matching errors will result in a small differential-mode output offset voltage. For the G = 1 case with a ground-referenced input signal and the output common-mode level set for 2.5 V, an output offset of as much as 25 mV (1% of the difference in common-mode levels) can result if 1% tolerance resistors are used. Resistors of 1% tolerance will result in a worst case input CMRR of about 40 dB, worst case differential mode output offset of 25 mV due to 2.5-V level-shift, and no significant degradation in output balance error.

The effective input impedance of a circuit, such as the one in Figure 6.33, at $V_{IN+}$ and $V_{IN–}$ will depend on whether the amplifier is being driven by a single-ended or differential signal source. For balanced differential input signals, the input impedance ($R_{IN,dm}$) between the inputs ( $V_{IN+}$ and $V_{IN–}$) is simply:

$$R_{INdm} = 2 \times R_G \qquad \text{Eq. 6.5}$$

In the case of a single-ended input signal (for example, if $V_{IN–}$ is grounded, and the input signal is applied to $V_{IN+}$), the input impedance becomes:

$$R_{IN,dm} = \left( \frac{R_G}{1 - \frac{R_F}{2 \times (R_G + R_F)}} \right) \qquad \text{Eq. 6.6}$$

The circuit's input impedance is effectively higher than it would be for a conventional op amp connected as an inverter, because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the input resistor $R_G$.

Figure 6.34 shows some of the possible configurations for the AD813x differential amplifier. Figure 6.34A is the standard configuration which utilizes two feedback networks, characterized by feedback factors β1 and β2, respectively. Note that each feedback factor can vary anywhere between 0 and 1.

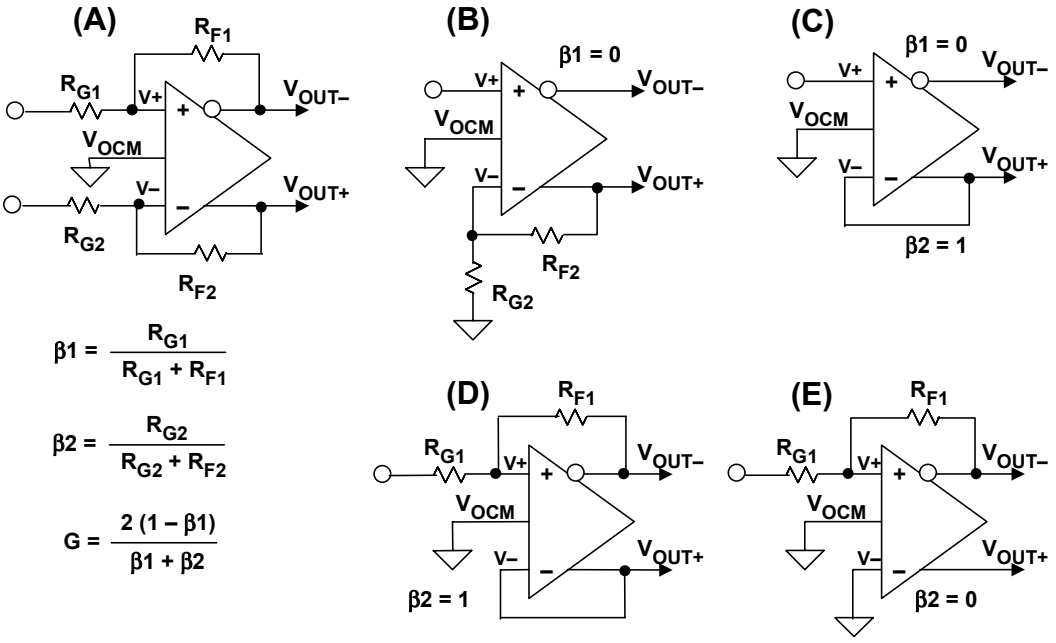



***Figure 6.34:*** *Some Configurations for Differential Amplifiers*

Figure 6.34B shows a configuration where there is no feedback from $V_{OUT-}$ to V+, i.e., β1 = 0. In this case, β2 determines the amount of $V_{OUT+}$ that is fed back to V–, and the circuit is similar to a non-inverting op amp configuration, except for the presence of the additional complementary output. Therefore, the overall gain is twice that of a non-inverting op amp, or $2 \times (1 + R_{F2}/R_{G2})$, or $2 \times (1/\beta 2)$.

Figure 6.34C shows a circuit where β1 = 0 and β2 = 1. This circuit is essentially provides a resistorless gain of 2.

Figure 6.34D shows a circuit where β2 = 1, and β1 is determined by $R_{F1}$ and $R_{G1}$. The gain of this circuit is always less than 2.

Finally, the circuit of Figure 6.34E has β2 = 0, and is very similar to a conventional inverting op amp, except for the additional complementary output at $V_{OUT+}$.

The AD813x-series are also well suited to balanced differential line driving as shown in Figure 6.35 where the AD8132 drives a 100-Ω twisted pair cable. The AD8132 is configured as a gain of 2 driver to account for the factor of 2 loss due to the source and load terminated cable. In this configuration, the bandwidth of the AD8132 is approximately 160 MHz.

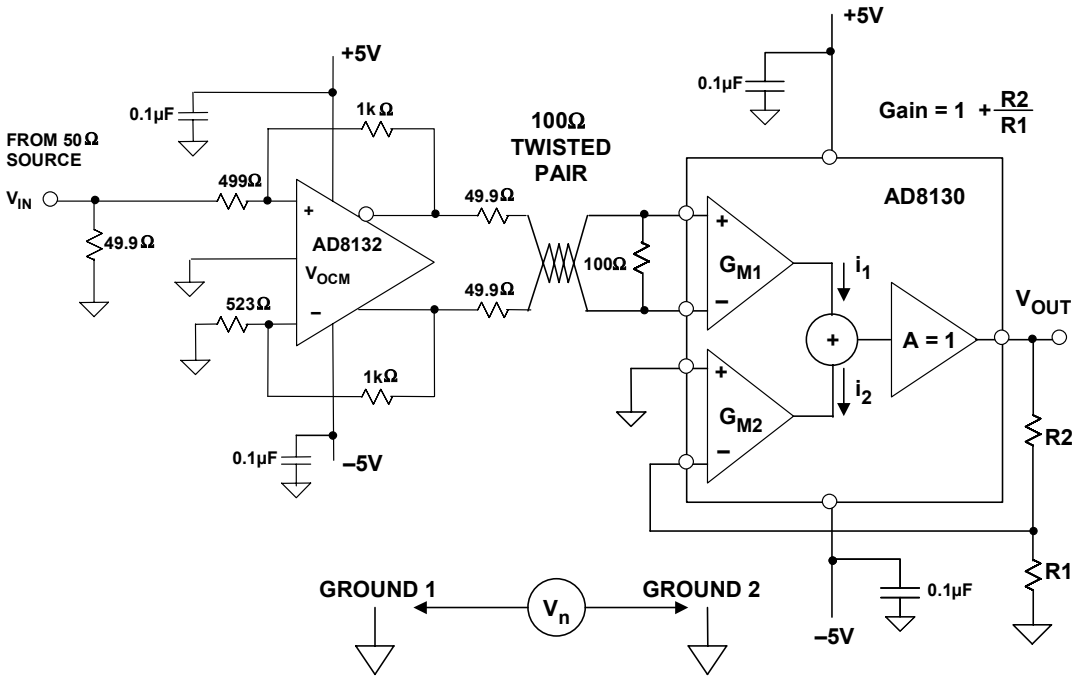



***Figure 6.35:*** *High Speed Differential Line Driver, Line Receiver Applications*

The line receiver is an AD8130 differential receiver which has a unique architecture called "active feedback" to achieve approximately 70-dB common-mode rejection at 10 MHz (Reference 10). For a gain of 1, the AD8130 has a 3-dB bandwidth of approximately 270 MHz.

The AD8130 utilizes two identical input transconductance ($g_m$) stages whose output currents are summed together at a high impedance node and then buffered to the output. The output currents of the two $g_m$ stages must be equal but opposite in sign, therefore, the respective input voltages must also be equal but opposite in sign. The differential input signal is applied to one of the stages ($G_{M1}$), and negative feedback is applied to the other ($G_{M2}$) as in a traditional op amp. The gain is equal to 1 + R2/R1. The $G_{M1}$ stage therefore provides a truly balanced input for the terminated twisted pair for the best common-mode rejection. Further details of operation of the AD8130 can be found in Reference 10.

**Driving Differential Input ADCs with Integrated Differential Drivers**

The AD8131, AD8132, AD8137, AD8138, and AD8139 differential ADC drivers are ideal replacements for transformer drivers when direct coupling is required. They can also provide the necessary gain and level shifting required to interface a bipolar signal to a high performance ADC input. In addition, the AD8137 has rail-to-rail outputs to simplify interfacing to low voltage differential input ADCs, and the AD8139 (also rail-to-rail output) is optimized for low noise and low distortion for 14- to 16-bit applications.

Figure 6.36 shows an application where the AD8137 differential amplifier is used as a level shifter and driver for the AD7450A 12-bit, 1-MSPS 3-V ADC (Reference 11). The AD7450A has fully differential inputs, and the input range is 4-V p-p differential when an external 2-V reference (ADR390) is applied. This implies that the signals at each output of the AD8137 driver must swing between +0.5 V and + 2.5 V (out of phase) when operating on a single 3-V supply. The rail-to-rail output structure of the AD8137 will provide this voltage swing with some safety margin. The +1.5-V common-mode voltage for the AD8137 is set by a resistive divider connected to the +3-V supply.

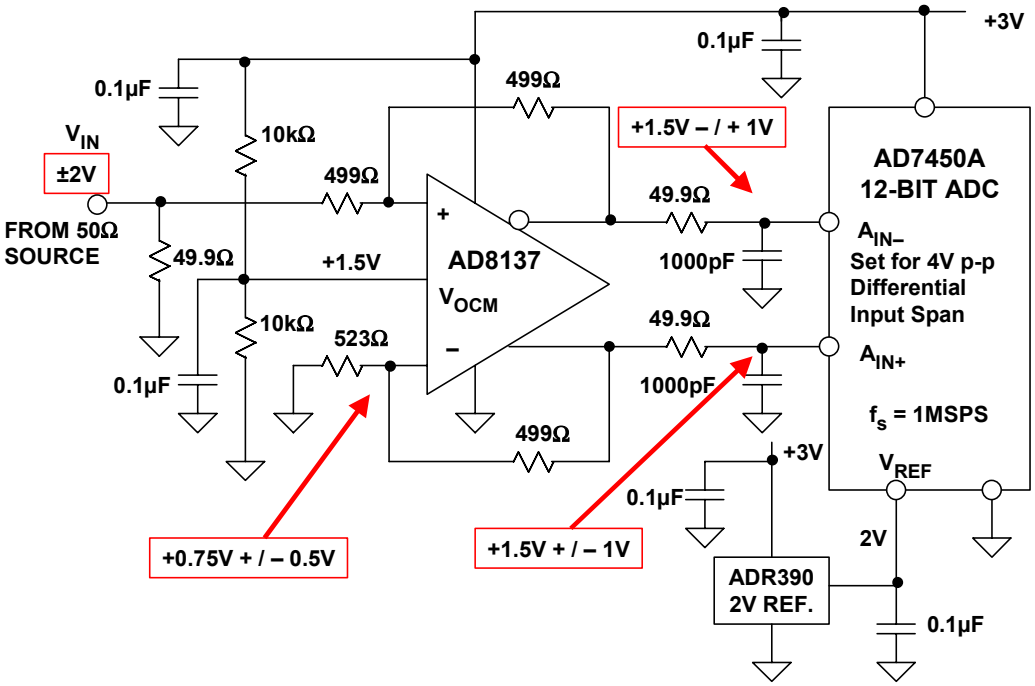



***Figure 6.36:*** *AD8137 Driving AD7450A 12-Bit, 1-MSPS, 3-V ADC*

The inputs to the AD8137 must swing between +0.25 V and +1.25 V. This is not a problem, since the input of the AD8137 is a differential PNP pair. The 523-Ω resistor from the inverting input to ground approximately balances the net feedforward resistance seen at the non-inverting input (499 Ω + 25 Ω = 524 Ω).

For higher frequency applications, the AD8138 differential amplifier has a 3-dB small-signal bandwidth of 320 MHz (G = +1) and is designed to give low harmonic distortion as an ADC driver. The circuit provides excellent output gain and phase matching, and the balanced structure suppresses even-order harmonics.

Figure 6.37 shows the AD8138 driving the AD9235 12-bit, 20-/40-/65-MSPS CMOS ADC (see Reference 12). This entire circuit operates on a single +3-V supply. A 1-V p-p bipolar single-ended input signal produces a 1-V p-p differential signal at the output of the AD8138, centered around a common-mode voltage of +1.5 V (mid-supply). The feedback network is chosen to provide a gain of 1, and the 523-Ω resistor from the inverting input to ground approximately balances the net feedforward resistance seen at the non-inverting input as in the previous example.

Each of the differential inputs of the AD8138 swings between +0.625 V and +0.875 V, and each output swings between +1.25 V and +1.75 V. These voltages fall within the allowable input and output common-mode voltage range of the AD8138 operating on a single +3-V supply. The output stage of the AD8138 is of the complementary emitter-follower type, and at least 1-V of headroom is required from either supply rail.

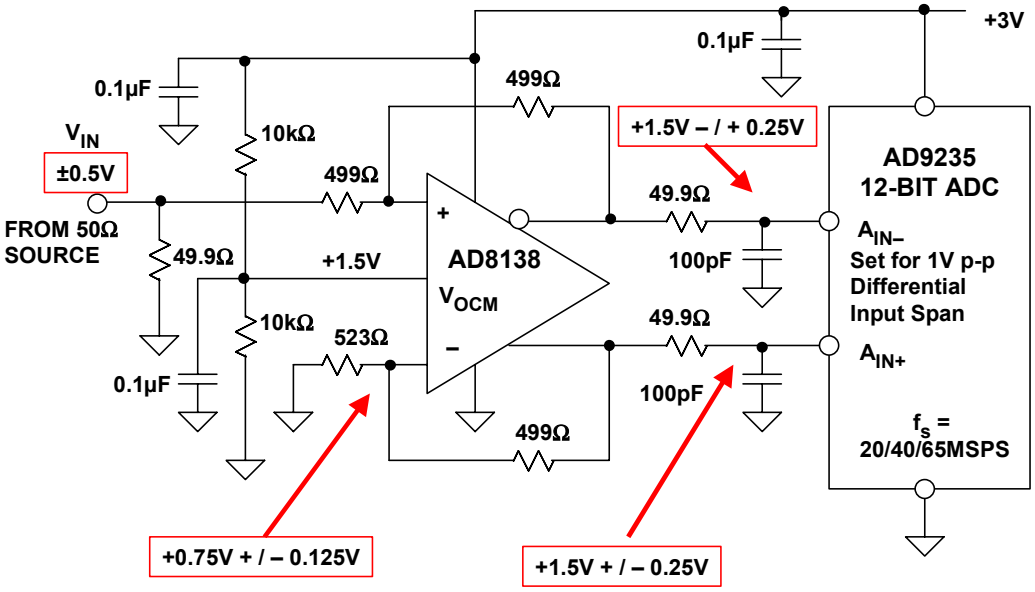



***Figure 6.37:*** *AD8138 Driving AD9235 12-Bit, 20-/40-/65-MSPS ADC*

It is important to understand the effects of the ADC driver on overall system noise. The circuit of Figure 6.37 will be used as an example, with the corresponding calculations shown in Figure 6.38. The output voltage noise spectral density of the AD8138 for a gain of 1 is 11.6 nV/√Hz (taken directly from the data sheet). This value includes the effects of input voltage noise, current noise, and resistor noise. To obtain the total rms output noise of the AD8138, the output noise spectral density is multiplied by the square root of the equivalent noise bandwidth of 50 MHz, which is set by the single-pole lowpass filters placed between the differential amplifier outputs and the ADC inputs.

Note that the closed-loop bandwidth of the AD8138 is 300 MHz, and the input bandwidth of the AD9235 is 500 MHz. With no filter, the output noise of the AD8138 would be integrated over the full 300-MHz amplifier closed-loop bandwidth. (In general, with no filtering, the amplifier noise must be integrated over either the amplifier closed-loop bandwidth or the ADC input bandwidth, whichever is less—or the geometric mean if the frequencies are close to each other).

However, the sampling frequency of the ADC is 65 MSPS, thereby implying that signals above 32.5 MHz are not of interest, assuming Nyquist operation (as opposed to undersampling applications where the input signal can be greater than the Nyquist frequency, $f_S/2$). The addition of this simple filter significantly reduces noise effects as will be demonstrated.

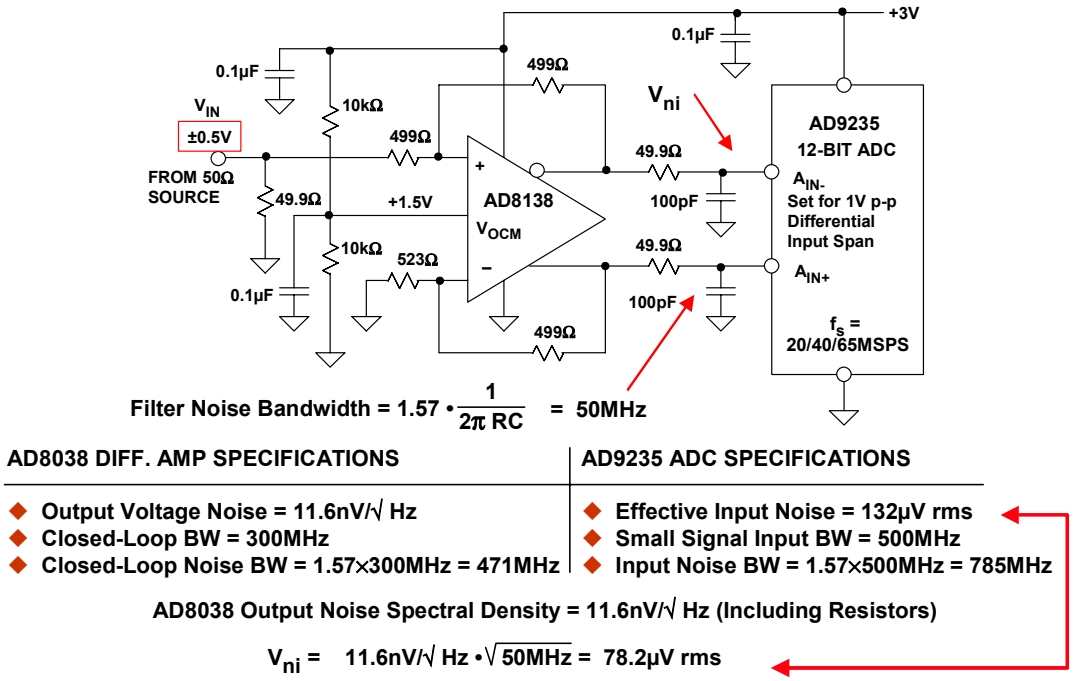



***Figure 6.38:*** *Noise Calculations for the AD8138 Differential Op Amp Driving the AD9235 12-Bit, 20-/40-/65-MSPS ADC*

The noise at the output of the lowpass filter, $V_{ni}$, is calculated to be approximately 78.2-µV rms which is only slightly more than half the effective input noise of the AD9235, 132-µV rms. The effective input noise of the AD9235 is specified as 0.54-LSB rms, which corresponds to (1 V / 4096)×(0.54) = 132-µV rms. Without the filter, the noise from the op amp would be integrated over the full 471-MHz closed-loop noise bandwidth of the AD8138 (1.57×300 MHz = 471 MHz ). This would yield a noise of 252-µV rms, compared to 78.2-µV rms obtained with lowpass filtering.

This serves to illustrate the general concept shown in Figure 6.39. In most high speed system applications, a passive antialiasing filter (either lowpass for baseband sampling, or bandpass for undersampling) is required, and placing this filter between the drive amplifier and the ADC can significantly reduce the noise contribution due to the amplifier. The filter therefore serves not only as an antialiasing filter but also as a noise filter for the amplifier. It should be noted, however, that if the filter is placed between the amplifier and the ADC, then the amplifier must be able to drive the impedance of the filter without significant distortion.

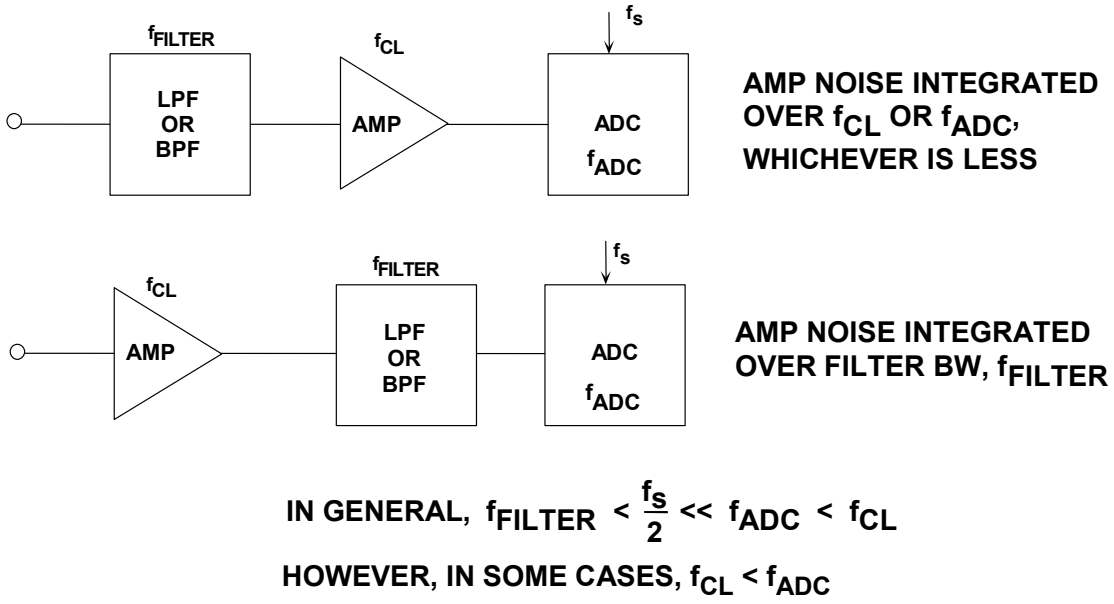



***Figure 6.39:*** *Proper Positioning of the Antialiasing Filter Will Reduce the Effects of Op Amp Noise*

High speed wide dynamic range ADCs such as the AD6645 14-bit 80-/105-MSPS ADC require very low noise, low distortion drivers, and RF transformers generally give optimum performance as previously described. However, there are applications where dc coupling is required, and this places an extremely high burden on the differential driver. Figure 6.40 shows the AD8139 differential driver operating as a dc-coupled level shifter as in the previous examples. The AD8139 has a rail-to-rail output stage, a bandwidth of 370 MHz, and a voltage noise of 2 nV/√Hz. SFDR is greater than 88 dBc for a 20-MHz, 2-V p-p output.

The AD6645 input common-mode voltage is set by its internal reference of +2.4 V, and this voltage is in turn applied to the AD8139 $V_{OCM}$ input pin. The outputs of the AD8139 swing between +1.85 V and +2.95 V, well within the common-mode output range of the amplifier.

Another RF/IF differential amplifier useful for an ac coupled driver for ADCs such as the AD6645 is the 2.2-GHz AD8351 (Reference 13). A typical application circuit is shown in Figure 6.41.

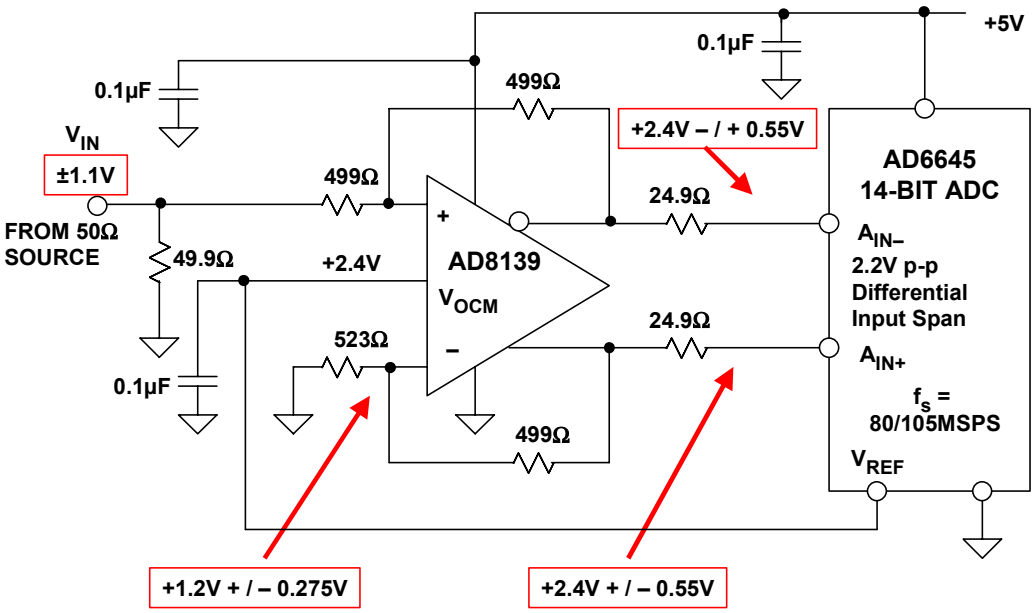
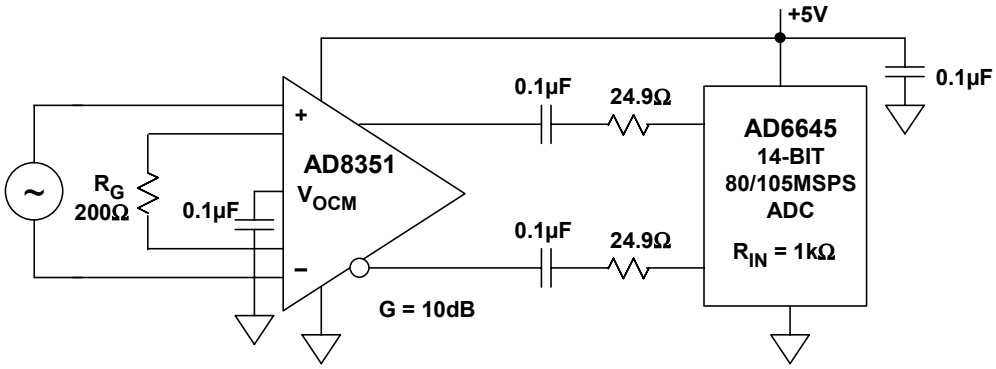



***Figure 6.40:*** *AD8139 Application as DC Coupled Driver for the AD6645 14-bit, 80-/105-MSPS ADC*




**AD8351 KEY FEATURES**

- **3dB Bandwidth: 2.2GHz for gain of 12dB**
- **Slew rate: 13,000V/µs**
- **Single resistor programmable gain, 0dB to 26dB**
- **Input noise: 2.7nV/√Hz**
- **Single supply: 3 to 5.5V**
- **Adjustable output common-mode voltage**

***Figure 6.41:*** *AD8351 Low Distortion Differential RF/IF Amplifier Application*

The AD8351 sets the standard in high performance, low distortion differential ADC drivers. It is ideal where additional low-noise gain is required ahead of the ADC. Gain is resistor programmable from 0 dB to 26 dB. Output common-mode voltage is set via the $V_{OCM}$ pin. The AD8351 input stage operates at a common-mode voltage of about +2.5 V and is not designed for dc coupling.

Typical performance data as a driver for the AD6645 is shown in Figure 6.42. The data was taken for a sampling rate of 80 MSPS with an input signal of 65 MHz. The undersampled 65-MHz signal appears in the FFT output spectrum at 15 MHz (80 MHz – 65 MHz = 15 MHz). The gain of the AD8351 is set for 10 dB, and the SFDR is 78.2 dBc.

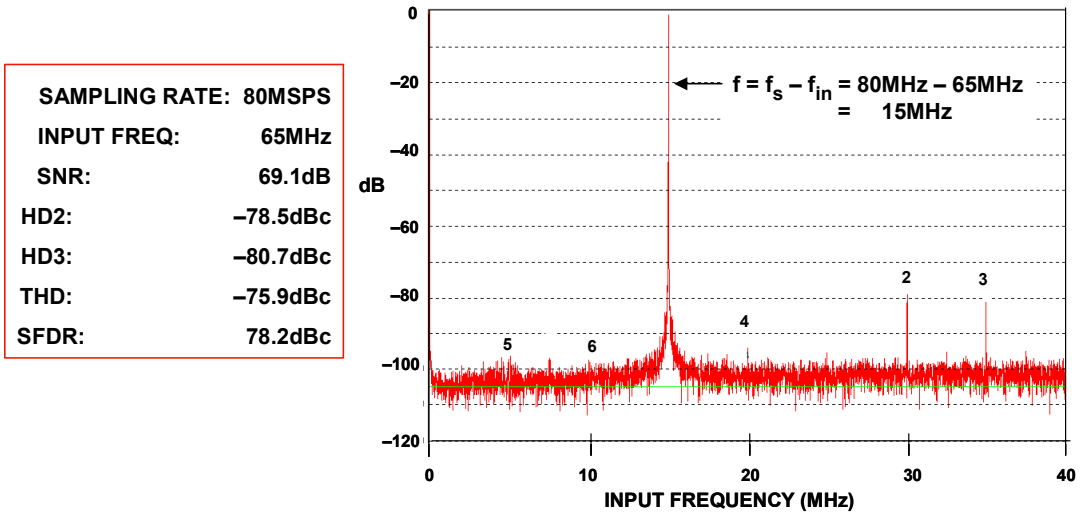



***Figure 6.42:*** *AD8351 Differential ADC Driver Performance with AD6645 ADC (G = 10 dB)*

The AD8351 can also be used as an ac-coupled single-ended to differential converter when working with single-ended signals as shown in the application circuit of Figure 6.43. The external resistors $R_F$ and $R_G$ are selected per the data sheet recommendations. Even though the differential balance is not perfect under these conditions, the SFDR for a 65-MHz input is reduced by only a few dB relative to the fully differential case shown in Figure 6.42.

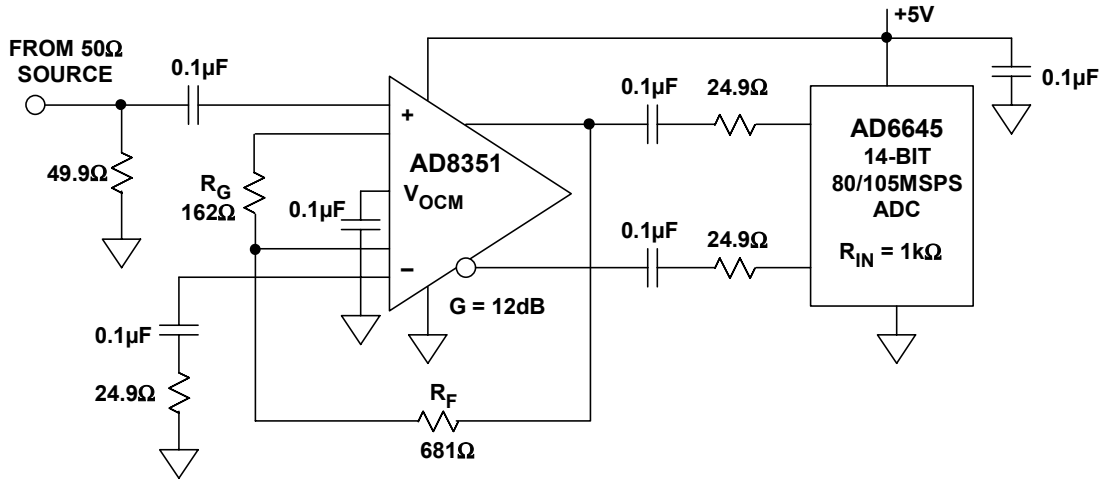



***Figure 6.43:*** *Using the AD8351 as a Single-Ended to Differential Converter*

For low distortion differential 12-bit ADC driver applications where programmable variable gain is required, the AD8370 digitally controlled variable-gain amplifier (VGA) is an excellent choice (Reference 14). Figure 6.44 shows the AD8370 as a single-ended to differential converter driving the AD9433 12-bit, 105-/125-MSPS BiCMOS ADC. The 3-dB bandwidth of the AD8370 is 700 MHz, and the gain is programmable over two ranges (–11 dB to + 17 dB and +6 dB to +34 dB) via a 3-wire serial interface. The AD8370 is designed for use at IF frequencies up to 380 MHz.

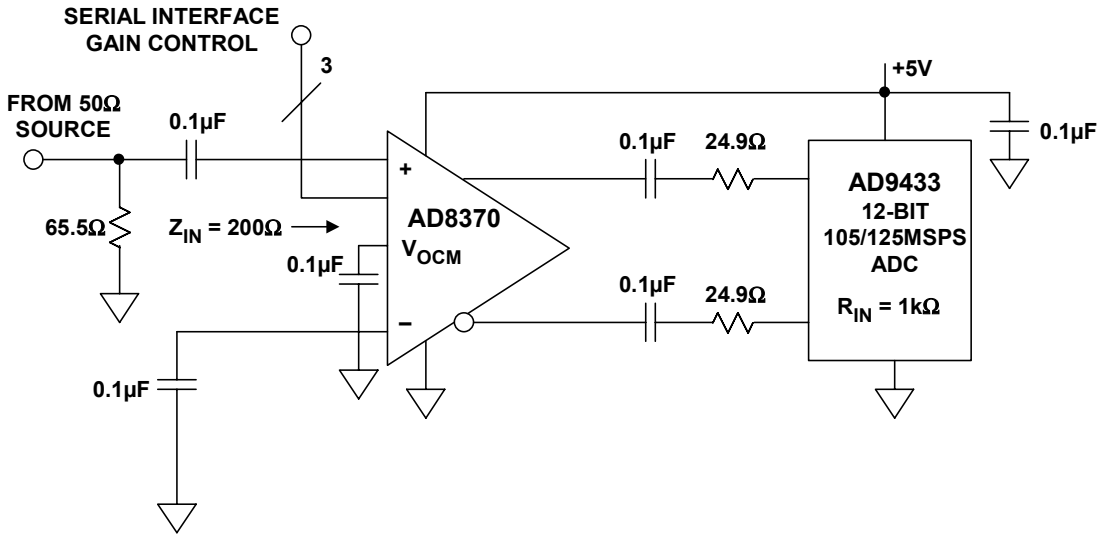



***Figure 6.44:*** *AD8370 Variable Gain Amplifier as a Low Distortion ADC Driver*

Driving low distortion high performance 16-bit ADCs such as the AD7677 16-bit, 1-MSPS ADC requires special care, especially with respect to noise and linearity. For example, the AD7677 has an INL specification of ±1 LSB, THD of –110 dB at 45 kHz, and 94-dB SINAD @ 45 kHz.

The AD7677 is a CMOS charge redistribution switched capacitor SAR design that operates on a single +5-V supply (Reference 15). Typical power dissipation is only 115 mW when operating at 1 MSPS. The converter is optimized for a differential drive input. Input referred noise is only 0.35-LSB rms, so a low noise drive amplifier is required. The AD8021 200-MHz op amp was especially designed with 16-bit systems in mind (Reference 16). Voltage noise is only 2.1 nV/√Hz, and distortion is less than 90 dBc for a 1-MHz output. The AD8021 also has dc precision with 1-mV maximum offset voltage, and 0.5-µV/°C drift. Quiescent current is 7 mA.

The low noise drive circuit in Figure 6.45 shows a single-ended to differential conversion using a pair of AD8021 op amps. The output common-mode voltage is set for +1.25 V by applying +1.25 V to the non-inverting input of the bottom AD8021. With no input filtering, the output noise of the differential driver must be integrated over the entire 16-MHz input bandwidth of the AD7677. This noise contribution can be reduced to approximately 0.13 LSB rms by the addition of a simple single-pole 4-MHz RC lowpass filter as shown.

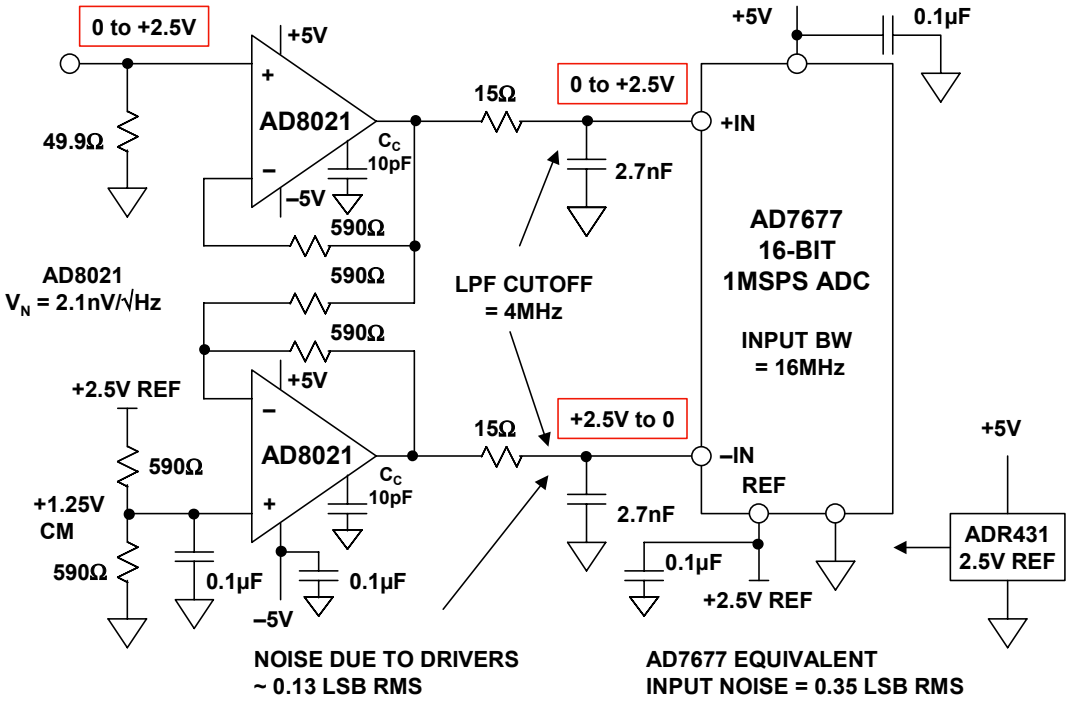



***Figure 6.45:*** *A True 16-bit ADC Requires a True 16-Bit Driver*

The circuit shown in Figure 6.45 will operate with excellent matching up to several MHz. However, the matching of the outputs can be extended to greater than 100 MHz by individually compensating the two AD8021 op amps as shown in Figure 6.46. The inverting and non-inverting bandwidths can be closely matched using this technique, thus minimizing distortion. This circuit illustrates an inverter-follower driver operating at a gain of 2, using individually compensated AD8021s.

The values of feedback and load resistors were selected to provide a total load of less than 1 kΩ, and the equivalent resistances seen at each op amp's inputs were matched to minimize offset voltage and drift. Figure 6.46 also shows the resulting ac responses of each half of the differential driver.

Rather than using the balanced AD8021 circuit (requiring two op amps), the AD8139 differential amplifier offers another alternative for driving 14/-16-/18-bit ADCs. Figure 6.47 shows the AD8139 driving the 18-bit, 800-kSPS AD7674 switched capacitor SAR ADC.

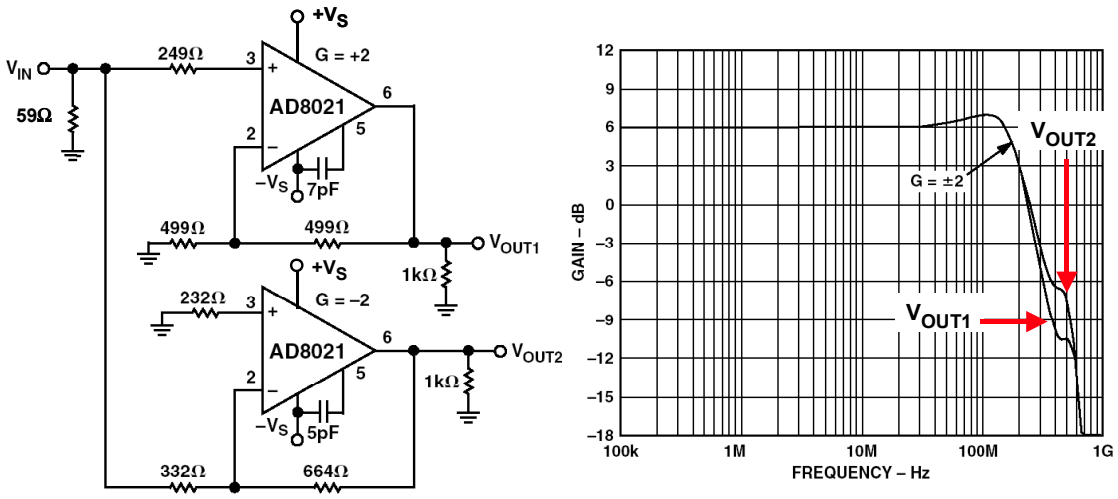



***Figure 6.46:*** *Balanced AD8021 Driver Compensated to Give Matched Gains to > 100 MHz*

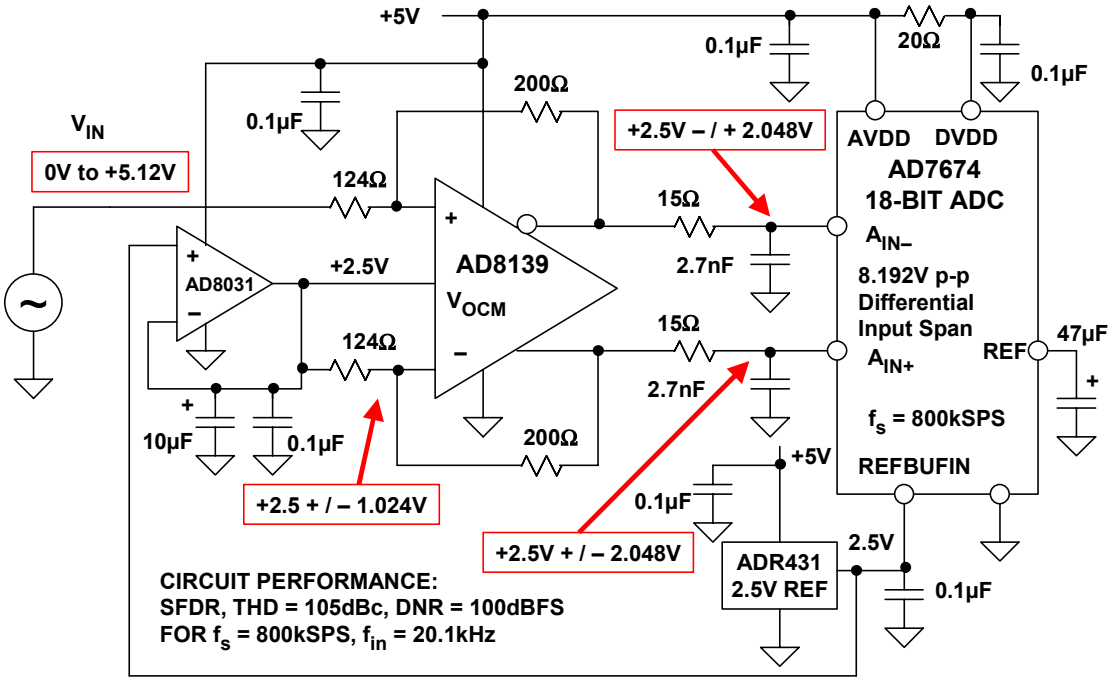



***Figure 6.47:*** *AD8139 Low Noise Differential Driver in a 18-bit ADC Application*

Applying a +2.5-V reference to the REFBUFIN pin of the AD7674 generates an internal reference voltage of +4.096 V. The input range of the ADC is then equal to 8.192 V p-p differential.

The circuit scales and level shifts the unipolar 0-V to +5.12-V input voltage to fit the range of the AD7674. The required gain of 1.6 is set by the ratio of the feedback to the feedforward resistor: 200 Ω/124 Ω = 1.6. The required common-mode voltage of +2.5 V is developed from the external ADR431 reference which also drives the AD7674 REFBUFIN. This voltage must be buffered by the AD8031 wideband op amp because of

the required sink/source current of approximately ±8.2 mA. The signals at the outputs of the AD8139 must swing from +0.5 V to +4.5 V (out of phase), which is within the range of the AD8139 operating on a single +5-V supply. The signals at the inputs of the AD8139 swing between +1.476 V and +3.524 V, which is well within the allowable input common-mode range when operating on a single +5-V supply.

As in the circuit previously shown in Figure 6.45, the 15-Ω resistors in conjuction with the 2.7-nF capacitors form a 4-MHz lowpass filter to the output noise of the AD8139.

# REFERENCES:
# 6.1 DRIVING ADC ANALOG INPUTS

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2. Data sheet for AD8057/AD8058 Low Cost, High Performance Voltage Feedback, 325 MHz Amplifiers, http://www.analog.com.

3. Chapter 8 of Walt Kester, Editor, Practical Design Techniques for Sensor Signal Conditioning, Analog Devices, 1999, ISBN: 0-916550-20-6. (Also available at http://www.analog.com).

4. Data Sheet for AD7466/AD7467/AD7468 1.6 V, Micropower 12-/10-/8-Bit ADCs in 6-Lead SOT-23, http://www.analog.com.

5. Data Sheet for AD7890 8-Channel, 12-Bit Serial, Data Acquisition System, http://www.analog.com.

6. Mini-Circuits, P.O. Box 350166, Brooklyn, NY, 11235, 718-934-4500, http://www.minicircuits.com.

7. Data Sheet for AD9430 12-Bit, 170 MSPS/210 MSPS 3.3 V A/D Converter, http://www.analog.com.

8. Data Sheet for AD6645 14-Bit, 80/105 MSPS A/D Converter, http://www.analog.com.

9. Data Sheets for AD8131, AD8132, AD8137, AD8138, AD8139 Differential Amplifiers, http://www.analog.com.

10. Data Sheets for AD830, AD8129, AD8130 Differential Receiver Amplifiers, http://www.analog.com.

11. Data Sheet for AD7450A/AD7440 Differential Input, 1 MSPS, 12- and 10-Bit ADCs in 8-Lead SOT-23, http://www.analog.com.

12. Data Sheet for AD9235 12-Bit, 20/40/65 MSPS 3 V A/D Converter, http://www.analog.com.

13. Data Sheet for AD8351 Low Distortion Differential RF/IF Amplifier, http://www.analog.com.

14. Data Sheet for AD8370 Digital Control VGA 700MHz Differential Amplifier, http://www.analog.com.

15. Data Sheet for AD7677 16-Bit, 1 LSB INL, 1 MSPS Differential ADC, http://www.analog.com.

16. Data Sheet for AD8021 Low Noise, High Speed Amplifier for 16-Bit Systems, http://www.analog.com.

# NOTES:

# SECTION 6.2: ADC AND DAC DIGITAL INTERFACES (AND RELATED ISSUES)

*Walt Kester*

## Introduction

A discussion of the broad area of data converter digital interfaces, timing, etc., can quickly become detailed and very tedious because of the many variations associated with specific products. We will therefore only attempt to point out the highlights in this section. While it is possible to generalize to some degree, the fact is that there is absolutely no substitute for careful study of the particular converter data sheet to clarify key points.

Modern data converters are much more digitally intensive than their predecessors of a few years ago. For example, high resolution Σ-Δ measurement ADCs typically have a number of internal control registers which are used to determine channel selection, set filter bandwidth, throughput rate, PGA gain, etc. These registers must be properly loaded by sending data to them via a serial interface port. This same serial port is often used to read the data out of the ADC at the end of a conversion cycle. Modern high frequency communications converters have also become digitally intensive. For instance, direct digital synthesis (DDS) ICs have internal registers which control the output frequency, amplitude, phase, type of modulation, etc.

There are other issues relating to the digital and timing portions of data converters, such as the condition of logic states immediately after power-on, the effect of pipeline delays, burst mode operation (some will, some won't), minimum sampling frequency, sleep and standby modes, etc.

Many of these topics are very similar to those encountered when designing with microprocessors, microcontrollers, and DSPs. However, successful designing with data converters not only requires understanding of digital and timing issues but also diligent attention to the analog design—layout, grounding, decoupling, etc. These hardware design topics are covered in considerable detail in Chapter 9 of this book.

## Power-On Initialization of Data Converters

When power is first applied to a simple flip flop—the fundamental digital storage element—there is generally no way to accurately predict what its output state will be. Without the addition of additional *power-on* circuitry or initialization procedures, the same is true of the many registers contained inside microprocessors, microcontrollers, DSPs, and of course, mixed signal devices such as ADCs and DACs.

While power-on reset features have been common with microprocessors, microcontrollers, and DSPs, such features are now included in some data converters—especially those which are highly digitally intensive, or where it is critical that signals be at certain levels after power-on.

A good example is a DAC that is used inside an industrial control loop. If the DAC is controlling an actuator, such as a vibration table, one can easily visualize a potential problem if the DAC analog output is fullscale at power-on. For this reason, many IC DACs used in industrial applications have internal power-on circuitry which forces the initial digital data into the DAC register (the register that controls the state of the DAC switches) to a known value (generally all 0's or mid-scale).

A digital potentiometer is another example of a device where the power-on state can be important. For this reason, some digital pots have on-chip non-volatile memory that stores the desired setting. Other digital pots without non-volatile memory usually have on-chip circuitry which forces the initial power-on value to either zero or mid-scale (the actual choice is pin selectable in some cases).

There is less reason to be concerned with the state of ADC outputs on power-on, because one is not generally interested in the ADC output until after a conversion command of some sort is applied. However, pipelined and Σ-Δ ADCs generally do require a number of sample clock cycles before the digital "pipeline" is flushed out and the output data is valid. Again, the data sheet for the device specifies this parameter.

## Initialization of Data Converter Internal Control Registers

Modern data converters, especially those which offer a high degree of functionality, often utilize internal control registers to set various operational parameters. For instance, the AD77xx family of Σ-Δ ADCs offer programmable throughput rate, filter cutoff frequency, amplifier gain, channel selection, etc. These parameters must be loaded into the ADC after power-on via a serial port. In order to ensure proper operation, these ADCs generally incorporate power-on reset and initialization circuitry which programs a known set of default values into the critical registers upon power-on. This allows the user to start system initialization with the ADC in valid operational state—an invaluable feature when troubleshooting an initial design at the PC board level.

In addition to the power-on reset feature, these types of ADCs generally have a separate reset pin which allows the converter to be put into a known state any time after power is connected. In some cases, the ADCs can also be reset to default conditions under software control.

Highly integrated DACs, Direct Digital Synthesis (DDS) systems, and many other mixed-signal ICs also have initialization features such as power-on reset, default modes, etc. As previously discussed, some have on-chip non-volatile memory which can be used to store the desired settings. The trend towards more integration and more programmability will ultimately lead to even more devices with on-chip volatile and non-volatile memory.

## Low Power, Sleep, and Standby Modes

In order to conserve power, especially in battery-powered applications, most modern data converters have some type of low-power, sleep, or standby mode, where the major portion of the internal circuitry is powered down—usually initiated by the application of

a signal to one of the pins, but sometimes under software control via internal control registers. In many applications where the converter is not required to operate continuously, this feature can lead to considerable power savings. Some converters have several reduced-power modes, depending upon the amount of circuitry to be shut down. In some cases, additional power savings can be achieved by disabling some or all of the external clocks.

Sleep-mode power supply current varies widely between devices, and can range from a few μA to tens of mA depending upon the normal-mode power dissipation. Recovery time from the sleep mode, or power-up time, is also a critical specification and can vary widely depending upon the device, but generally is in the order of a few μs to 100 μs.

During the sleep mode, power is maintained on critical internal mode-controlling registers, etc., however the conversion process is usually disabled. If the converter is pipelined or has internal digital filters (such as Σ-Δ ADCs or certain DACs with internal digital filters), a sufficient number of clock cycles must be allowed after power-up to flush out the pipelines before output data is valid.

## Single-Shot Mode, Burst Mode, and Minimum Sampling Frequency

This brings up an interesting timing issue with respect to pipelined ADCs which is not specifically related to the digital interface, but has a direct bearing on the application—the ability (or lack thereof) to operate at very low sampling rates, the burst mode, or the single-shot mode.

Many early successive approximation ADCs, such as the industry-standard AD574, were designed with internal clock generators that were triggered upon the receipt of an external *convert-start* signal. At the end of the conversion cycle, the signal on an output line (labeled *busy*, *conversion complete*, *data ready*, etc.) was asserted, indicating that the data was valid and that the conversion was complete. This type of ADC can be utilized in the single-shot mode, burst mode, or operated continuously, with no significant effect on performance. Many modern successive approximation ADCs require that the user supply a continuous high frequency clock (which controls the various steps in the conversion process) as well as the traditional *convert-start* pulse to initiate the actual conversion. The *convert-start* pulse can be synchronous or asynchronous with the high frequency clock in many converters. As long as the user supplies a continuous high frequency clock, these types of ADCs can generally be operated in the single-shot or burst mode.

It should be noted that this is one of the fundamental reasons why SAR ADCs are still so popular in data acquisition, especially multi-channel systems where an analog multiplexer drives the ADC. A single convert-start command yields the corresponding data—with no pipeline delay—thereby making it easy to identify the output data corresponding to a particular channel and clock pulse.

On the other hand, pipelined ADCs (see Chapter 3 of this book for detailed descriptions) require a number of sample clocks after power-on before the pipeline is cleared, and valid data appears at the output. In addition, the cascaded internal sample-and-hold amplifiers act as analog delay lines, and they are typically controlled by one or both phases of the actual sampling clock. That is, the "1" state of the sampling clock places some of the

SHAs in the *track* mode, and the others in the *hold* mode. The "0" state of the sampling clock reverses the track/hold states of the SHAs. The direct or indirect utilization of the sampling clock phases to control all internal operations reduces chip area, cost, and improves performance by eliminating additional internal clocks which could easily increase overall ADC noise and distortion were they to become noisy because of stray coupling from other parts of the circuit.

However, one can see that as the sampling frequency is decreased, the *hold* time of the SHAs increases proportionally—at some point, the *droop* (caused by leakage current flowing into or out of the hold capacitor) associated with the long hold times will produce large errors in the conversion, thereby rendering the output data invalid. In addition, internal circuits may enter saturation. Therefore, pipelined ADCs often have a *minimum* specified sampling frequency as well as the traditional maximum.

Although most pipelined ADCs cannot be directly operated in the single-shot or burst mode, they can be operated with a continuous sampling clock, and the output data gated to correspond with the desired sampling intervals.

Much more could be said about the topics discussed so far, but the reader should at least now be aware of some of the important issues that only a through study of the data sheet can clarify. The same can be said about the following section on the digital interface itself.

- **Power-on Reset and Initialization**
  - **DACs and Digital Pots**
  - **ADCs with Internal Control Registers**
  - **Default Conditions**
  - **Pipelined ADCs**
- **Low Power, Sleep, Standby Modes**
  - **Power Savings**
  - **Recovery or Power-Up Time**
- **Single-Shot, Burst Mode, and Minimum Sampling Frequency**
  - **SAR ADCs**
  - **Pipelined ADCs**
- **Get to Know Your Friendly Data Sheet!**
  - **"Getting to know you, getting to know all about you …"**
    **"Anna," from Rogers and Hammerstein's, *The King and I***

***Figure 6.48:*** *Some Important Digital and Timing Interface Issues for Data Converters*

## ADC Digital Output Interfaces

Early ADCs typically provided parallel output data interfaces. As resolutions increased, and microprocessors, microcontrollers, DSPs, became widespread, the serial interface became popular. Today, most 12-bit or greater ADCs which operate at or above 10 MSPS typically have a parallel output data interface, while low frequency high-resolution Σ-Δ measurement ADCs almost exclusively utilize a serial interface. In between these two sampling frequency ranges, one finds a wide variety of ADCs—some with parallel, some with serial, and some with options for both parallel and serial output data interfaces.

### ADC Serial Output Interfaces

Serial interfaces are typically 3-wire (sometimes 2-wire), and therefore there is a big savings in package pin count and cost versus the parallel interface, especially with high resolution ADCs. It is also very convenient to provide serial outputs on SAR-based and Σ-Δ ADCs since their conversion architecture is essentially serial. If an ADC is operating continuously, the period of the sampling clock must be long enough to transfer all the serial data across the interface at the interface data rate, with some appropriate amount of headroom. For instance, a 16-bit, 1-MSPS sampling ADC requires a serial output data rate of at least 16 MHz, which would not be a problem with most modern microprocessors, microcontrollers, or DSPs.

Most 3-wire serial interfaces associated with ADCs and DACs are compatible with standard serial interfaces such as SPI®,QSPI™, MICROWIRE™, and DSPs. Figure 6.49 shows the timing diagram for a typical serial output converter, the AD7466 12-bit, 200 kSPS ADC which is packaged in a 6-lead SOT-23 package.

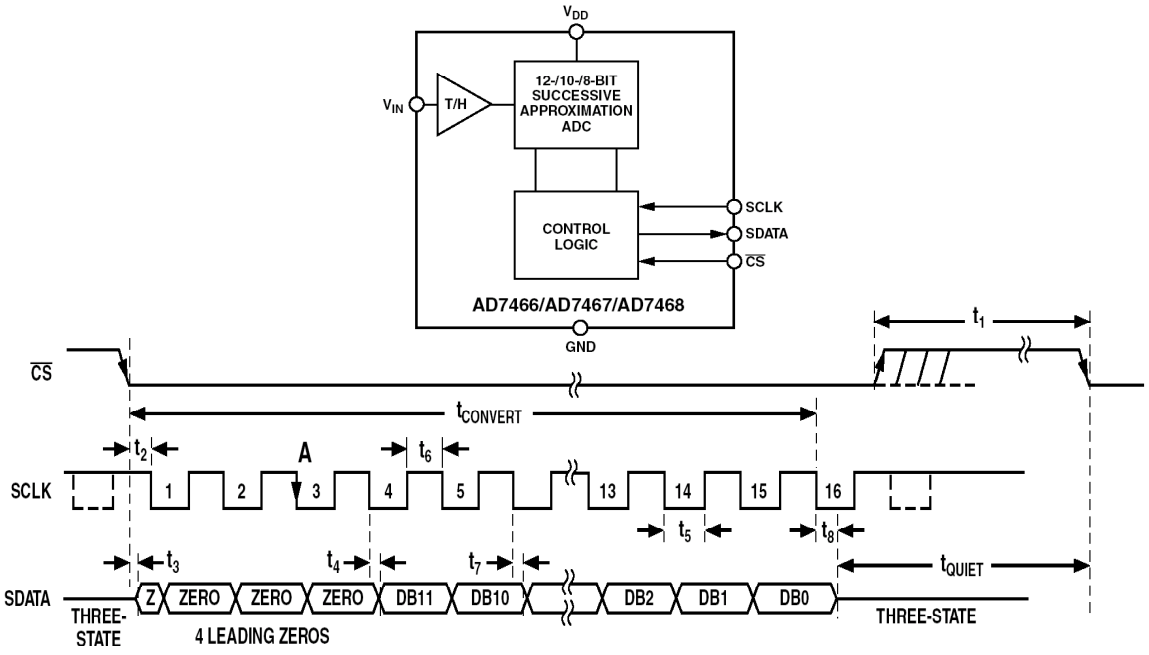



***Figure 6.49:*** *AD7466 12-Bit, 200-kSPS Serial Output Data Timing Diagram*

The AD7466 is normally in the power-down mode with the $\overline{CS}$ signal high. The part begins to power up on the $\overline{CS}$ falling edge. The falling edge of $\overline{CS}$ puts the track-and-hold into the track mode and takes the bus out of three-state. The conversion is also initiated at this point. On the third SCLK falling edge after the $\overline{CS}$ falling edge, the part should be fully powered up, as shown in Figure 6.49 at point "A," and the track-and-hold will return to hold. For the AD7466, the SDATA line will go back into three-state, and the part will enter power-down on the 16$^{th}$ SCLK falling edge. If the rising edge of $\overline{CS}$ occurs before 16 SCLKs have elapsed, the conversion will be terminated, the SDATA line will go back into three-state, and the part will enter power-down; otherwise SDATA returns to three-state on the 16$^{th}$ SCLK falling edge, as shown in Figure 6.49. Sixteen serial clock cycles are required to perform the conversion process and to access data from the AD7466.

$\overline{CS}$ going low provides the first leading zero to be read in by the microcontroller or DSP. The remaining data is then clocked out by subsequent SCLK falling edges, beginning with the second leading zero; thus the first clock falling edge on the serial clock has the first leading zero provided and also clocks out the second leading zero. For the AD7466, the final bit in the data transfer is valid on the 16$^{th}$ SCLK falling edge, having been clocked out on the previous (15$^{th}$) SCLK falling edge. In applications with a slow SCLK, it is possible to read in data on each SCLK rising edge. In such a case, the first falling edge of SCLK after the $\overline{CS}$ falling edge will clock out the second leading zero and could be read in the following rising edge. If the first SCLK edge after the $\overline{CS}$ falling edge is a falling edge, the first leading zero that was clocked out when $\overline{CS}$ went low will be missed unless it is not read on the first SCLK falling edge. The 15$^{th}$ falling edge of SCLK will clock out the last bit and it could be read in the following rising SCLK edge. If the first SCLK edge after $\overline{CS}$ falling edge is a rising edge, $\overline{CS}$ will clock out the first leading zero as before, and it may be read on the SCLK rising edge. The next SCLK falling edge will clock out the second leading zero, and it could be read on the following rising edge.

Looking at higher speed applications, LVDS (low voltage differential signaling) interfaces can be as high as 800 Mbits/s, thereby making serial data transfer practical even for some high speed ADCs. For instance, the AD9289 quad 12-bit, 65-MSPS ADC uses four serial LVDS outputs, each operating at 780 Mbits/s. A functional block diagram of the quad ADC is shown in Figure 6.50 (also see Reference 2).

The AD9229 is a quad 12-bit, 65-MSPS ADC converter with an on-chip track-and-hold circuit and is designed for low cost, low power, small size and ease of use. The converter operates up to 65-MSPS conversion rate and is optimized for outstanding dynamic performance where a small package size is critical. The ADC requires a single +3-V power supply and CMOS/TTL sample rate clock for full performance operation. No external reference or driver components are required for many applications. A separate output power supply pin supports LVDS-compatible serial digital output levels. The ADC automatically multiplies the sample rate clock for the appropriate LVDS serial data rate. An MSB trigger is provided to signal a new output byte. Power down is supported, and the ADC consumes less than 3 mW when enabled. A timing diagram is shown in Figure 6.51.

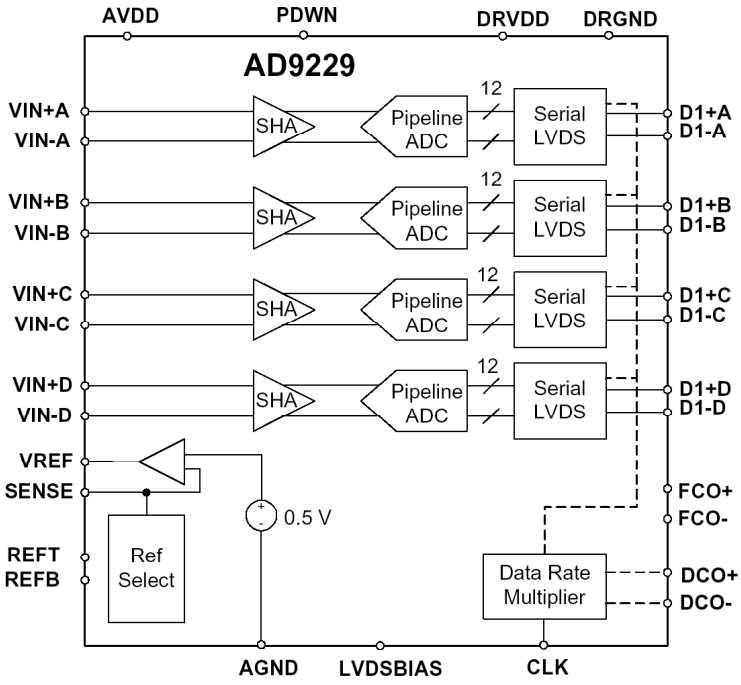



***Figure 6.50:*** *AD9229 Quad 12-Bit, 65-MSPS ADC with Serial LVDS Outputs*

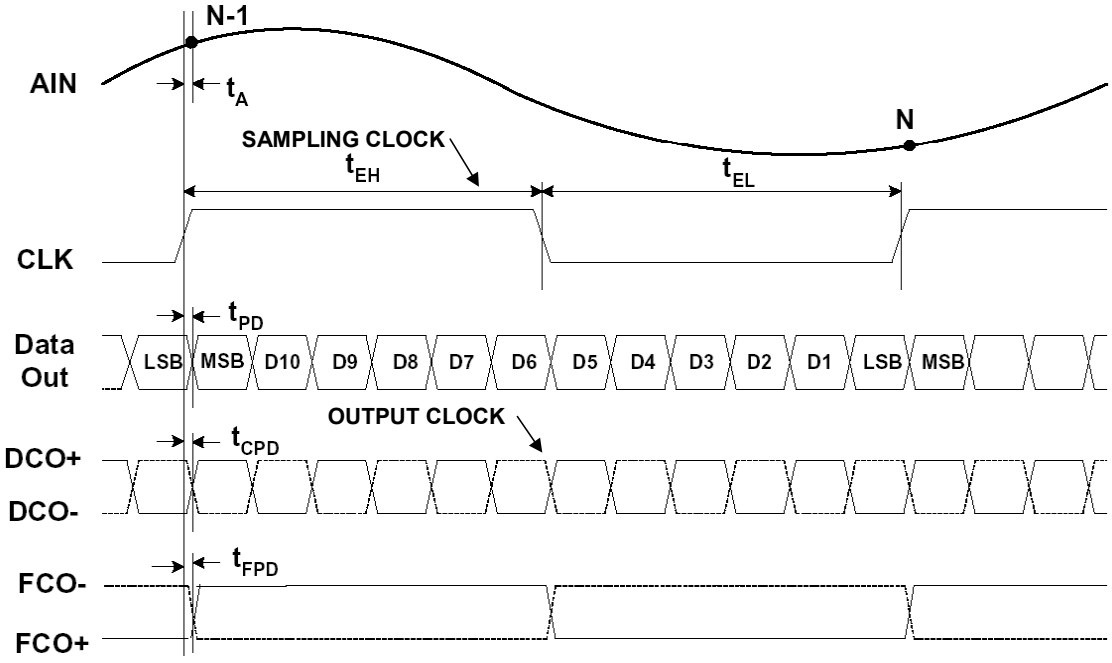



***Figure 6.51:*** *AD9289 Quad 8-Bit, 65-MSPS ADC*
*Serial LVDS Output Data Timing*

Data from each ADC is serialized and provided on a separate channel. The data rate for each serial stream is equal to 12-bits times the sample clock rate, with a maximum of 780 MHz (12-bits × 65 MSPS = 780 MHz). The lowest typical conversion rate allowable is 10 MSPS (recall that minimum sampling frequency specifications are characteristic of CMOS pipelined ADCs). Two output clocks are provided to assist in capturing data from the AD9289. The data clock out (DCO) is used to clock the output data and is equal to 6 times the sampling clock (CLK) rate.

Data is clocked out of the AD9229 on the rising and falling edges of DCO. The MSB clock (FCO) is used to signal the MSB of a new output byte and is equal to the sampling clock rate.

The use of high-speed serial LVDS data outputs in the AD9229 results in a huge savings in the pin count, compared with parallel outputs. A total of 48 data pins would be required to provide 4 individual parallel 12-bit single-ended CMOS outputs. Using serial LVDS, the AD9289 requires only 4 differential LVDS data outputs, or 8 pins, thereby saving a total 40 pins. In addition, the use of LVDS rather than CMOS reduces digital output transient currents and the overall ADC noise. A typical LVDS output driver designed in CMOS is shown in Figure 6.52. Further details regarding the LVDS specification can be found in Chapter 9 of this book.

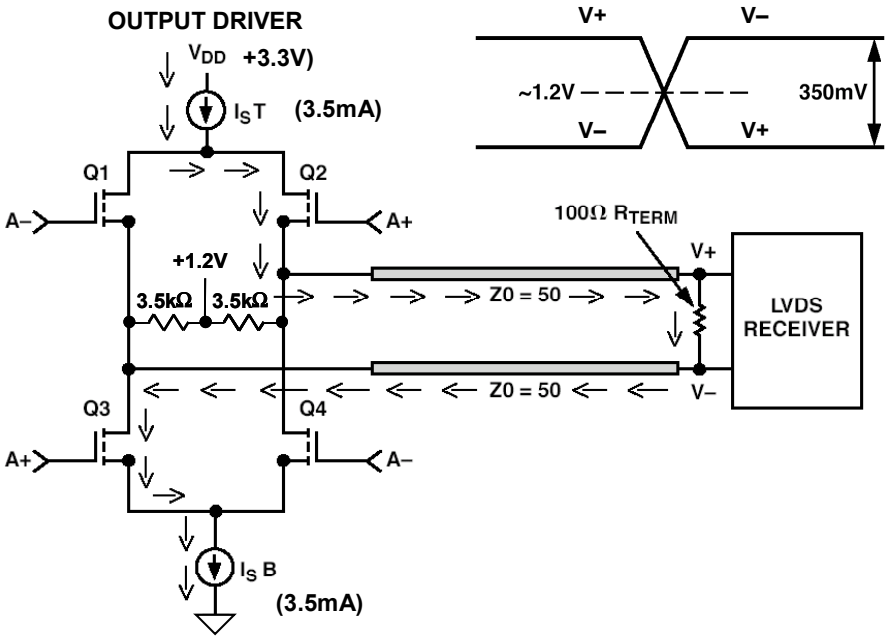



***Figure 6.52:*** *LVDS Driver Designed in CMOS*

**ADC Serial Interface to DSPs**

Because of its simplicity and efficiency, the serial interface has become a very popular way to interface ADCs and DACs to DSPs, and real-time operation is possible in many instances. We will consider a typical example of such an interface between a general purpose ADC and a fixed-point DSP.

The AD7853/AD7853L is a 12 bit, 200-/100-kSPS ADC which operates on a single +3-V to +5.5-V supply and dissipates only 4.5 mW (+3-V supply, AD7853L). After each conversion, the device automatically powers down to 25 μW. The AD7853/AD7853L is based on a successive approximation architecture and uses a charge redistribution (switched capacitor) DAC. A calibration feature removes gain and offset errors. A block diagram of the device is shown in Figure 6.53 (for more details, see Reference 3).

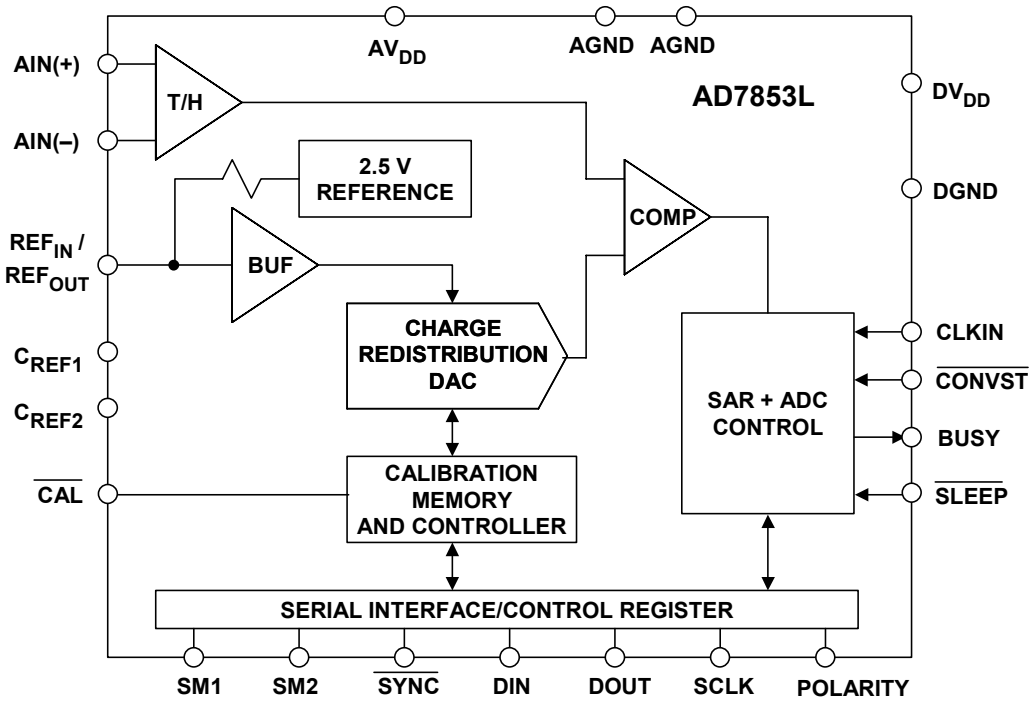



***Figure 6.53:*** *AD7853/AD7853L +3-V Single-Supply 12-Bit 200-/100-kSPS Serial Output ADC*

The AD7853 operates on a 4-MHz maximum external clock frequency. The AD7853L operates on a 1.8-MHz maximum external clock frequency. The timing diagram for AD7853L is shown in Figure 6.54. The AD7853/AD7853L has modes which configure the $\overline{\text{SYNC}}$ and SCLK as inputs or outputs. In the example shown here they are outputs generated by the AD7853L. The AD7853L serial clock operates at a maximum frequency of 1.8 MHz (556-ns period). The data bits are valid 330 ns after the positive-going edges of SCLK. This allows a setup time of approximately 330 ns minimum before the negative-going edges of SCLK, easily meeting the ADSP-2189M 4-ns $t_{SCS}$ requirement. The hold-time after the negative-going edge of SCLK is approximately 226 ns, again easily meeting the ADSP-2189M 7-ns $t_{SCH}$ timing requirement. These simple calculations show that the data and RFS setup and hold requirements of the ADSP-2189M are met

with considerable margin. For a much more detailed discussion of the serial interface timing between ADCs, DACs, and DSPs see Reference 5.

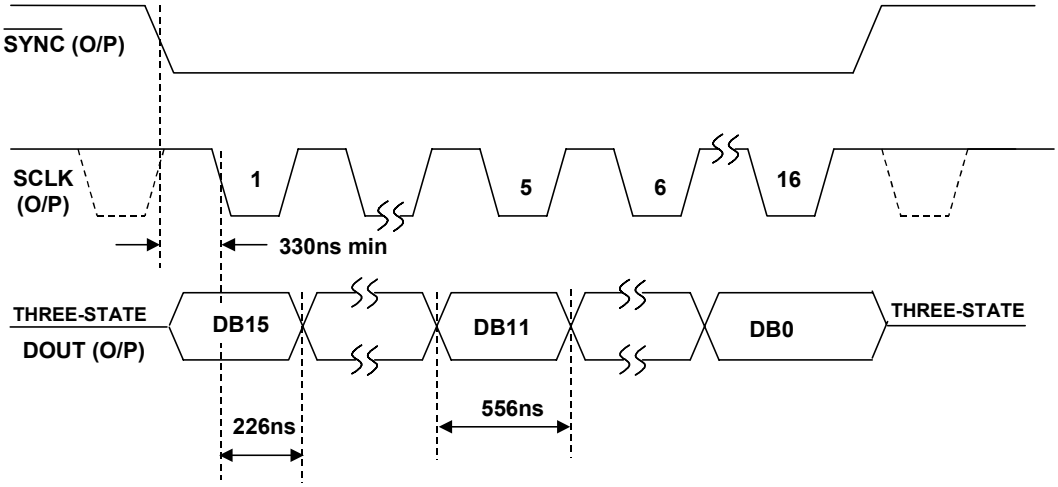



***Figure 6.54:*** *AD7853L Serial ADC Output Timing +3-V Supply, SCLK = 1.8 MHz*

Figure 6.55 shows the AD7853L interfaced to the ADSP-2189M connected in a mode to transmit data from the ADC to the DSP (alternate/master mode). The AD7853/AD7853L contains internal registers which can be accessed by writing from the DSP to the ADC via the serial port. These registers are used to set various modes in the AD7853/AD7853L as well as to initiate the calibration routines. These connections are not shown in the diagram.

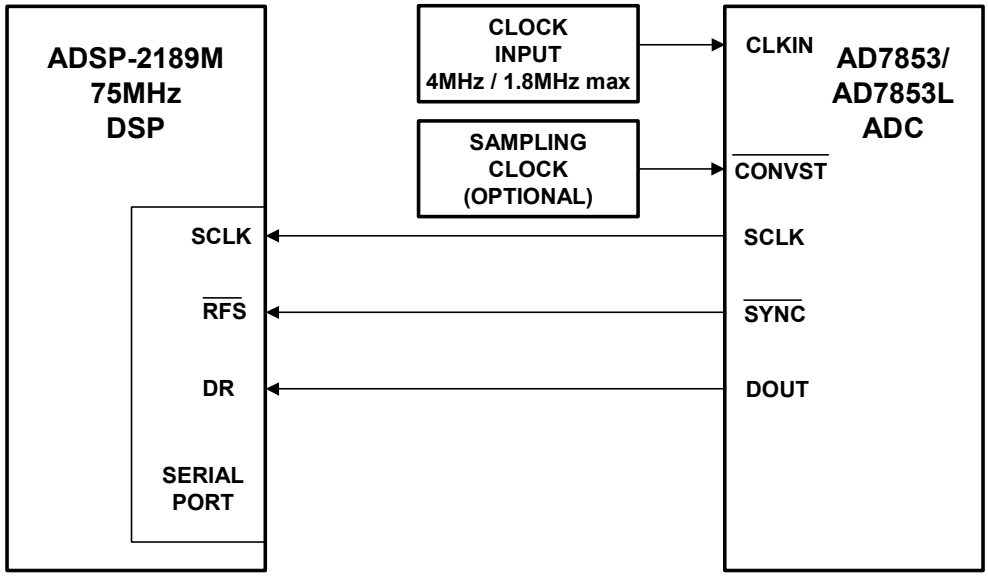



***Figure 6.55:*** *Interfacing the AD7853/AD7853L Serial Output ADCs to the ADSP-2189M DSP*

## ADC Parallel Output Interfaces

Parallel ADC output interfaces are popular, straightforward, and must be used when the product of sampling rate and resolution exceeds the capacity available serial links. For instance, using a maximum LVDS serial data link of 600 Mbits/s requires parallel data transmission for resolutions/sampling rates greater than 8 bits at 75 MSPS, 10 bits at 60 MSPS, 12 bits at 50 MSPS, 14 bits at 43 MSPS, 16 bits at 38 MSPS, etc.

Parallel ADC interface timing is relatively straightforward. At some specified time relative to the assertion of the appropriate edge of the sampling clock, the output data is valid. This time is specified on the data sheet, and may or may not be indicated by a *data ready*, or *data valid* output from the ADC. Also, the data appearing at the output may correspond to a previously applied sampling clock edge due to the pipeline delay of the ADC. In most cases, the output data is valid for an entire sampling clock period (neglecting the rise and fall times). Some parallel output ADCs have a *chip enable* function which allows the data outputs to be connected to a data bus, and the outputs are three-state until the chip enable is asserted by an external DSP, microcontroller, or microprocessor. However, there are general precautions that must be taken when connecting this type of output to a data bus—the most important is to ensure that there is no activity on the bus during the actual ADC conversion interval. Otherwise, bus activity may couple back into the ADC via the stray pin capacitance and corrupt the conversion. In addition, if the capacitive load of the bus is significant, there may be additional ADC digital output transients which can corrupt the conversion.

We will use the AD9430 12-bit, 170-/210-MSPS ADC to illustrate the timing associated with a modern high speed parallel output device (Reference 6). An overall block diagram of the AD9430 is shown in Figure 6.56. Notice that this ADC offers two output data options: demultiplexed CMOS outputs on two ports (each at one-half the sampling rate) or differential LVDS outputs at the full sampling rate. There is no penalty in pin count by providing these two options, because demuxed single-ended outputs on two ports require the same number of pins as differential LVDS outputs on a single port.

Figure 6.57 shows the AD9430 timing when using the LVDS output mode.
The AD9430 operates on an LVDS-compatible differential sampling clock which passes through internal *clock management* circuitry that stabilizes the duty cycle and thereby removes the sensitivity of the conversion process to variations in input sampling clock duty cycle.

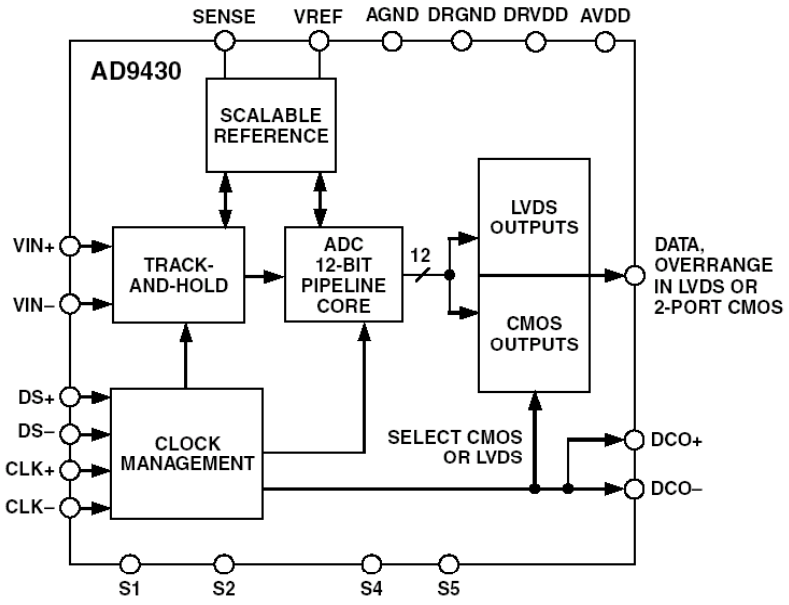



***Figure 6.56:*** *AD9430 12-Bit, 170-/210-MSPS ADC with LVDS or Demuxed CMOS Output Data Options*

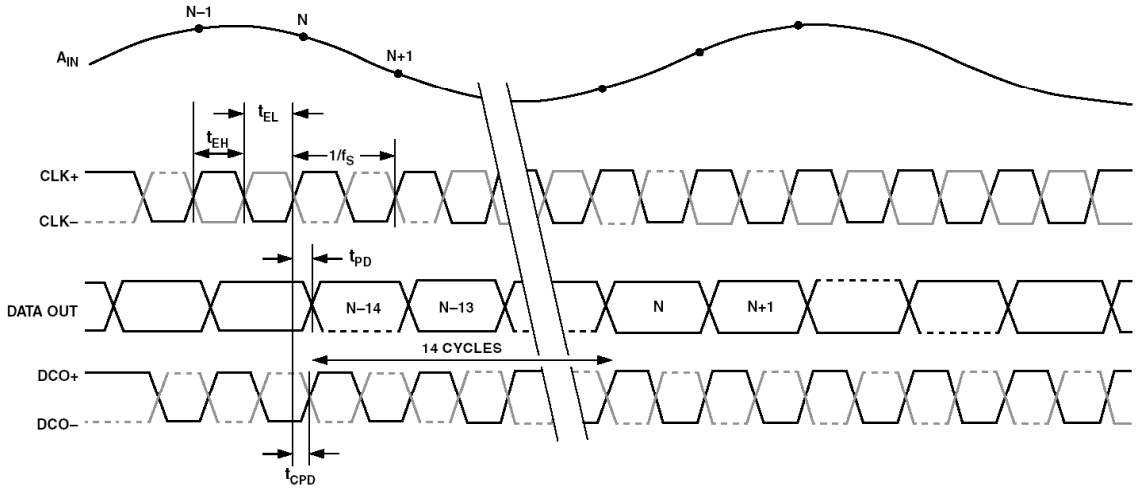



***Figure 6.57:*** *AD9430 LVDS Output Data Timing*

If the sampling frequency is known, the timing diagram in conjunction with the associated specifications for $t_{PD}$ and $t_{CPD}$ can be used to predict when the output data is valid with respect to either the positive-going edge of the sampling clock (CLK+) or the positive-going or negative-going edge of the data output clock (DCO+).

Because of the high 210-MSPS sampling rate (period = 4.76 ns), it is critical that both the ADC output timing and the receiver input timing be carefully examined so that the receiving register or memory can be clocked when the output data is stable. This "window" is short, and in the case of the AD9430, a *data valid* time of 2-ns minimum is guaranteed. ADC output timing, PC board trace delay and the input register (usually an FPGA) setup and hold time specifications all factor into determining the proper timing for a particular design, and great care must be taken in the analysis to ensure valid data is obtained.

Although best distortion and noise performance is obtained in the LVDS mode, the AD9430 can also be operated in the CMOS data output mode, in which case the output data is demultiplexed and available on 2 output ports at one-half the overall ADC sampling rate. The timing diagram for the CMOS mode is shown in Figure 6.58. Note that data is available in either interleaved or parallel format, depending upon the option selected.

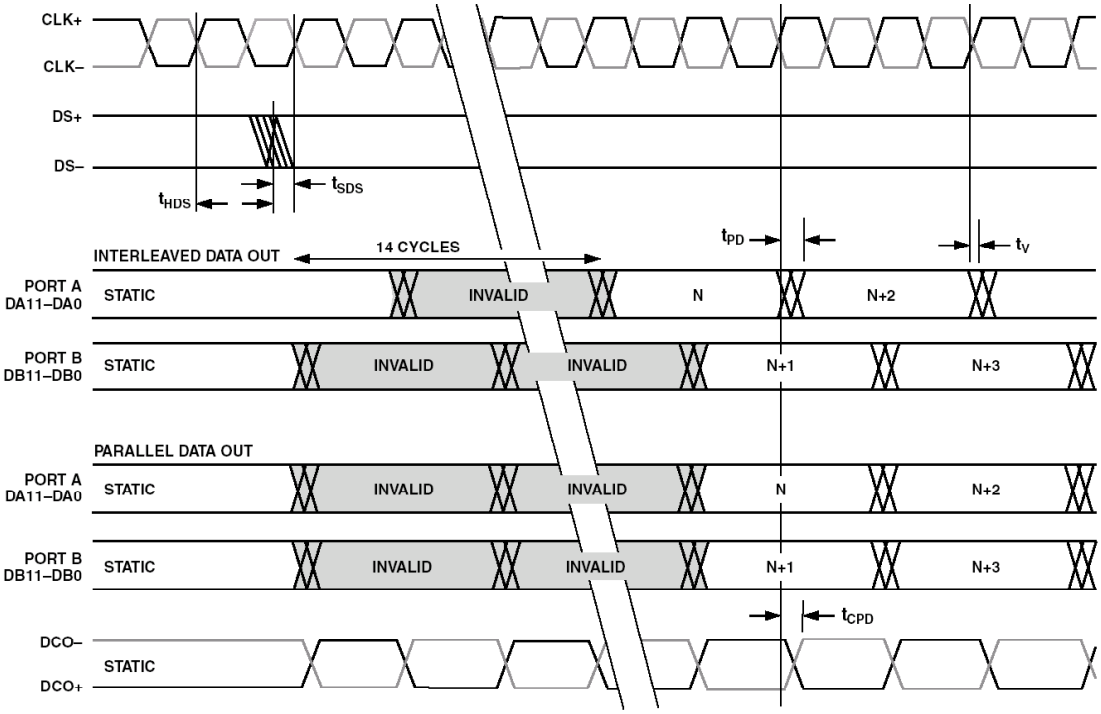



***Figure 6.58:*** *AD9430 Demuxed CMOS Output Data Timing*

High speed ADCs such as the AD9430 typically interface to an FPGA or buffer memory. Lower speed parallel output ADCs can interface directly to microcontrollers or DSPs via a standard parallel data bus. A good example is the AD7854/AD7854L 3-V, 12-bit, 200-/100-kSPS parallel output ADC (Reference 7). This device uses a successive approximation architecture based on a charge redistribution (switched capacitor) DAC. A calibration mode removes offset and gain errors. A block diagram of this general purpose converter is shown in Figure 6.59.

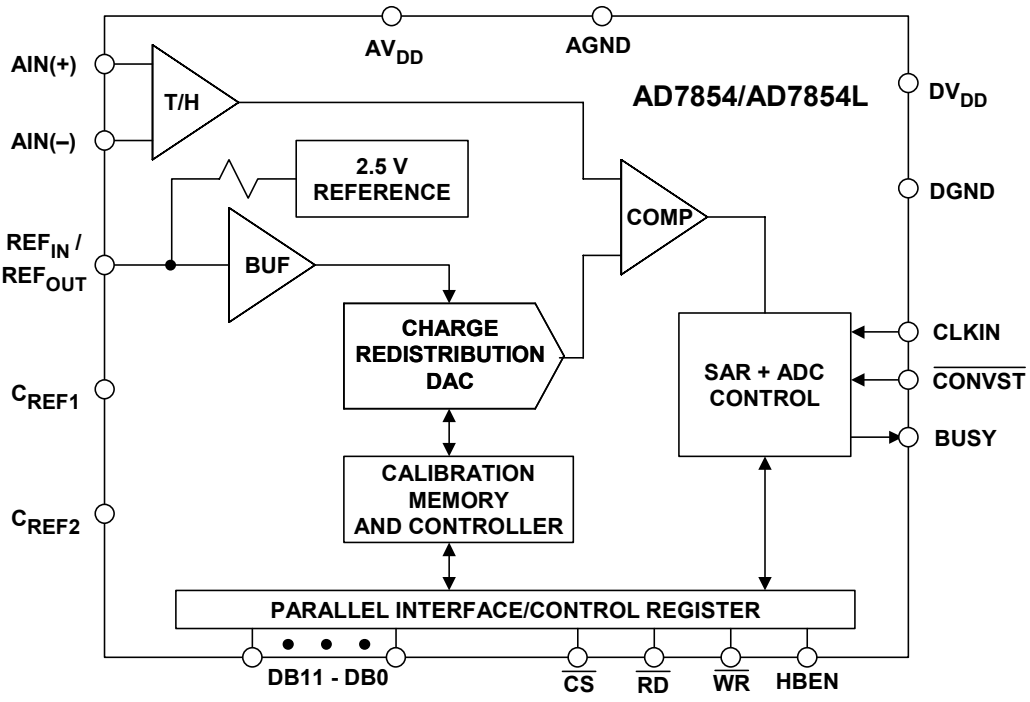



***Figure 6.59:*** *AD7854/AD7854L, +3-V Single Supply, 12-bit, 200-/100-kSPS Parallel Output ADC*

A simplified interface diagram for interfacing the AD7854/AD7854L to the ADSP-2189 75-MHz DSP is shown in Figure 6.60. This configuration allows the DSP to write data into the ADC parallel interface control register as well as to read data from the ADC. In normal operation, data is read from the ADC. The assertion of the $\overline{\text{CONVST}}$ signal initiates the conversion process. At the end of the conversion, the assertion of the ADC BUSY line acts as an interrupt signal to the DSP (applied to the DSP $\overline{\text{IRQ}}$ input). The DSP then reads the ADC output data using the $\overline{\text{CS}}$ and $\overline{\text{RD}}$ pins of the AD7854.

The 5 software wait states are required to widen the $\overline{\text{RD}}$ signal from the DSP so that it is compatible with the AD7854 ADC requirements. This process is a standard way of reading data from memory-mapped peripheral devices and is described in much more detail in Reference 5.

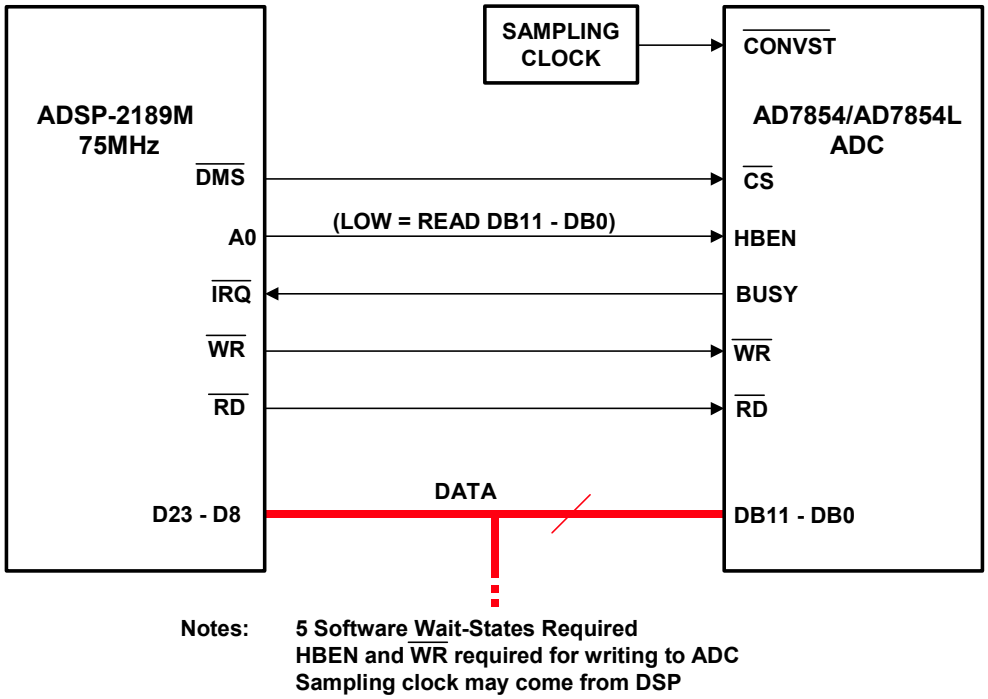



***Figure 6.60:*** *AD7854/AD7854L ADC Parallel Interface to ADSP-2189M*

## DAC Digital Input Interfaces

The earliest monolithic DACs contained little, if any, logic circuitry, and parallel data had to be maintained on the digital input to maintain the digital output. Today almost all DACs have input latches, and data need only be written once, not maintained.

There are innumerable variations in DAC input structures which will not be discussed here, but the majority today are "double-buffered." A double-buffered DAC has two sets of latches. Data is initially latched in the first rank and subsequently transferred to the second as shown in Figure 6.61. There are three reasons why this arrangement is useful.

The first is that it allows data to enter the DAC in many different ways. A DAC without a latch, or with a single latch, must be loaded with all bits at once, in parallel, since otherwise its output during loading may be totally different from what it was or what it is to become. A double-buffered DAC, on the other hand, may be loaded with parallel data, serial data, or with 4-bit or 8-bit words, or whatever, and the output will be unaffected until the new data is completely loaded and the DAC receives its update instruction.

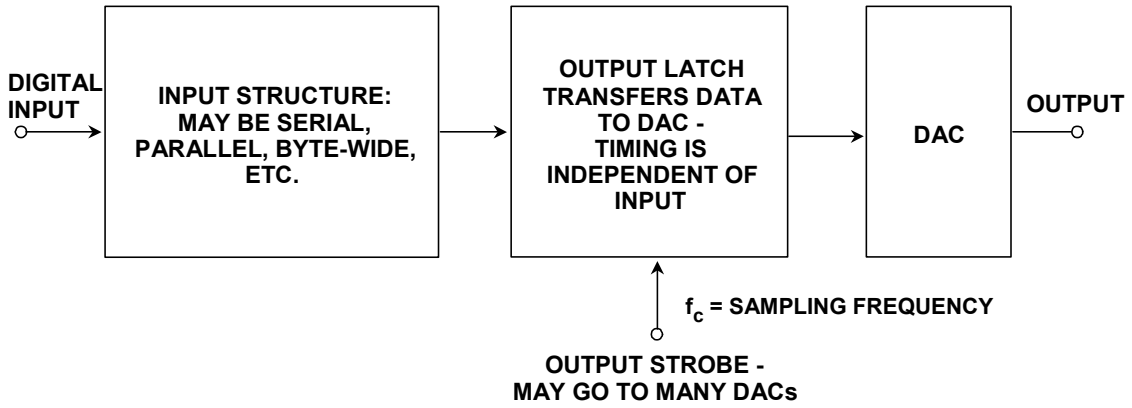



***Figure 6.61:*** *Double-Buffered DAC Permits Complex Input Structures and Simultaneous Update*

The second feature of this type of input structure is that the output clock can operate at a fixed frequency (the DAC update rate), while the input latch can be loaded asynchronously. This is useful in real-time signal reconstruction applications.

The third convenience of the double-buffered structure is that many DACs may be updated simultaneously: data is loaded into the first rank of each DAC in turn, and when all is ready, the output buffers of all DACs are updated at once. There are many DAC applications where the output of several DACs must change simultaneously, and the double-buffered structure allows this to be done very easily.

Most early monolithic high resolution DACs had parallel or byte-wide data ports and tended to be connected to parallel data buses and address decoders and addressed by microprocessors as if they were very small write-only memories (some DACs are not write-only, but can have their contents read as well—this is convenient for some ATE applications but is not very common). A DAC connected to a data bus is vulnerable to capacitive coupling of logic noise from the bus to the analog output. Many DACs today have serial data structures and are less vulnerable to such noise (since fewer noisy pins are involved), use fewer pins, and therefore take less space, and are frequently more convenient for use with modern microprocessors, many of which have serial data ports. Some, but not all, of such serial DACs have data outputs as well as data inputs so that several DACs may be connected in series and data clocked to them all from a single serial port. The arrangement is referred to as "daisy-chaining".

**DAC Serial Input Interfaces to DSPs**

Interfacing serial input DACs to the serial ports of DSPs such as the ADSP-21xx family is also relatively straightforward and similar to the previous discussion regarding serial output ADCs. The details will not be repeated here, but a simple interface example will be shown.

The AD5322 is a 12-bit, 100-kSPS dual DAC with a serial input interface (Reference 8). It operates on a single +2.5-V to +5.5-V supply, and a block diagram is shown in Figure 6.62. Power dissipation on a +3-V supply is 690 µW. A power-down feature reduces this

to 0.15 μW. Total harmonic distortion is greater than 70 dB below full scale for a 10-kHz output. The references for the two DACs are derived from two reference pins (one per DAC). The reference inputs may be configured as buffered or unbuffered inputs. The outputs of both DACs may be updated simultaneously using the asynchronous $\overline{\text{LDAC}}$ input. The device contains a power-on reset circuit that ensures that the DAC outputs power up to 0 V and remain there until a valid write takes place to the device.

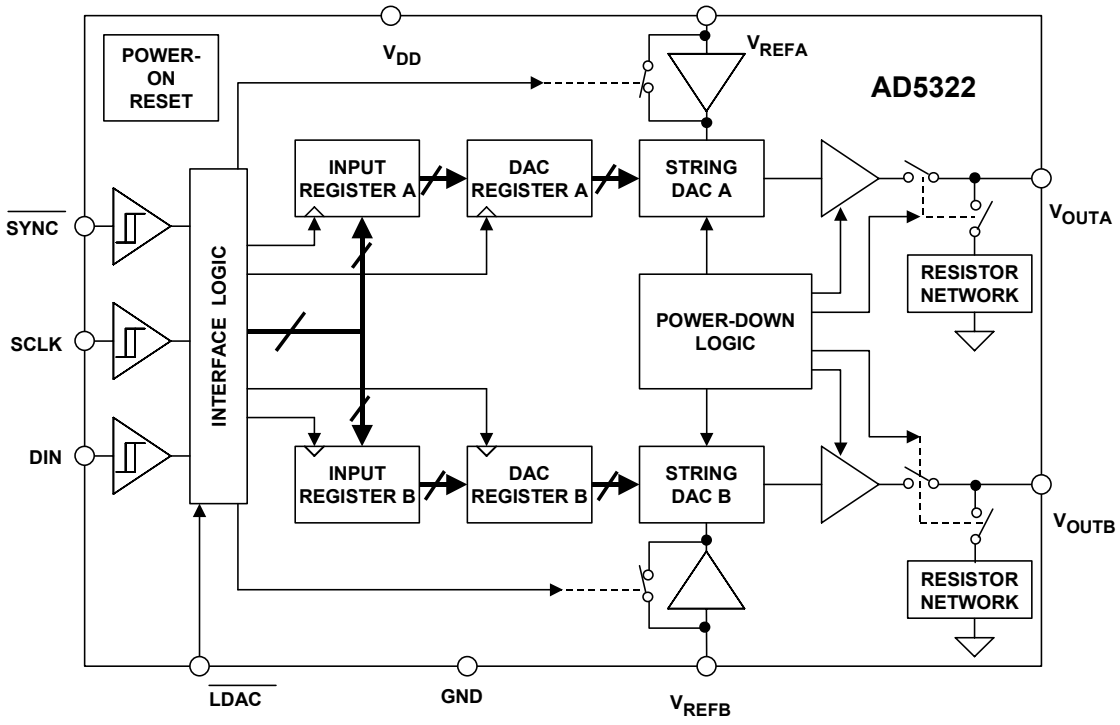



***Figure 6.62:*** *AD5322 12-BIT, 100-kSPS Dual Serial DAC*

Data is normally input to the AD5322 via the SCLK, DIN, and $\overline{\text{SYNC}}$ pins from the serial port of the DSP. When the $\overline{\text{SYNC}}$ signal goes low, the input shift register is enabled. Data is transferred into the AD5322 on the falling edges of the following 16 clocks. A typical interface between the ADSP-2189M and the AD5322 is shown in Figure 6.63. Notice that the clocks to the AD5322 are generated from the ADSP-2189M clock. It is also possible to generate the SCLK and $\overline{\text{SYNC}}$ signals externally to the AD5322 and use them to drive the ADSP-2189M. The serial interface of the AD5322 is not fast enough to handle the ADSP-2189M maximum master clock frequency. However, the serial interface clocks are programmable and can be set to generate the proper timing for fast or slow DACs.

The input shift register in the AD5322 is 16-bits wide. The 16-bit word consists of four control bits followed by 12 bits of DAC data. The first bit loaded determines whether the data is for DAC A or DAC B. The second bit determines if the reference input will be buffered or unbuffered. The next two bits control the operating modes of the DAC (normal, power-down with 1 kΩ to ground, power-down with 100 kΩ to ground, or power-down with a high impedance output).

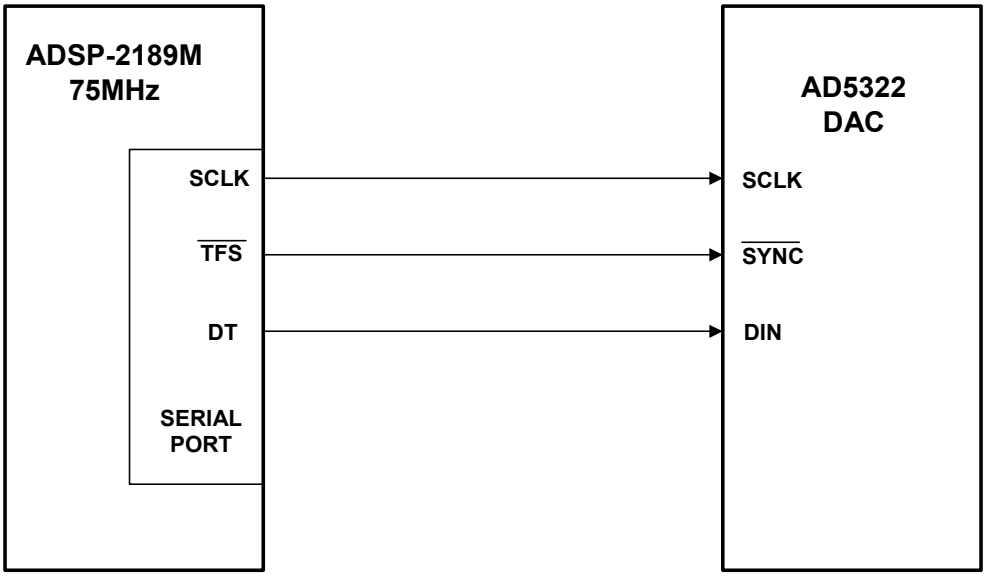



***Figure 6.63:*** *AD5322 DAC Serial Interface to ADSP-2189M*

**DAC Parallel Input Interfaces to DSPs**

The AD5340 is a 12-bit 100-kSPS DAC which has a parallel data interface. It operates on a single +2.5-V to +5.5-V supply and dissipates only 345µW (+3-V supply). A power-down mode further reduces the power to 0.24 µW. The part incorporates an on-chip output buffer which can drive the output close to both supply rails. The AD5340 allows the choice of a buffered or unbuffered reference input. The device has a power-on reset circuit that ensures that the DAC output powers on at 0 V and remains there until valid data is written to the part. A block diagram is shown in Figure 6.64. The input is double buffered.

A method for interfacing the AD5340 to a DSP is shown in Figure 6.65. The sampling clock to the DAC updates the internal DAC register via the $\overline{\text{LDAC}}$ input. The sampling clock also generates an interrupt signal to the DSP's $\overline{\text{IRQ}}$ input, thereby requesting a new data word. After the DSP computes the next data word, it puts the word on the data bus and transfers it to the DAC input register via the DAC's $\overline{\text{CS}}$ and $\overline{\text{WR}}$ inputs. Note that this configuration allows real time operation, provided the DSP outputs the new data word before the next sampling clock occurs. The 2 additional software wait states are required to widen the $\overline{\text{WR}}$ signal from the DSP so that it meets the requirements of the AD5340 DAC.

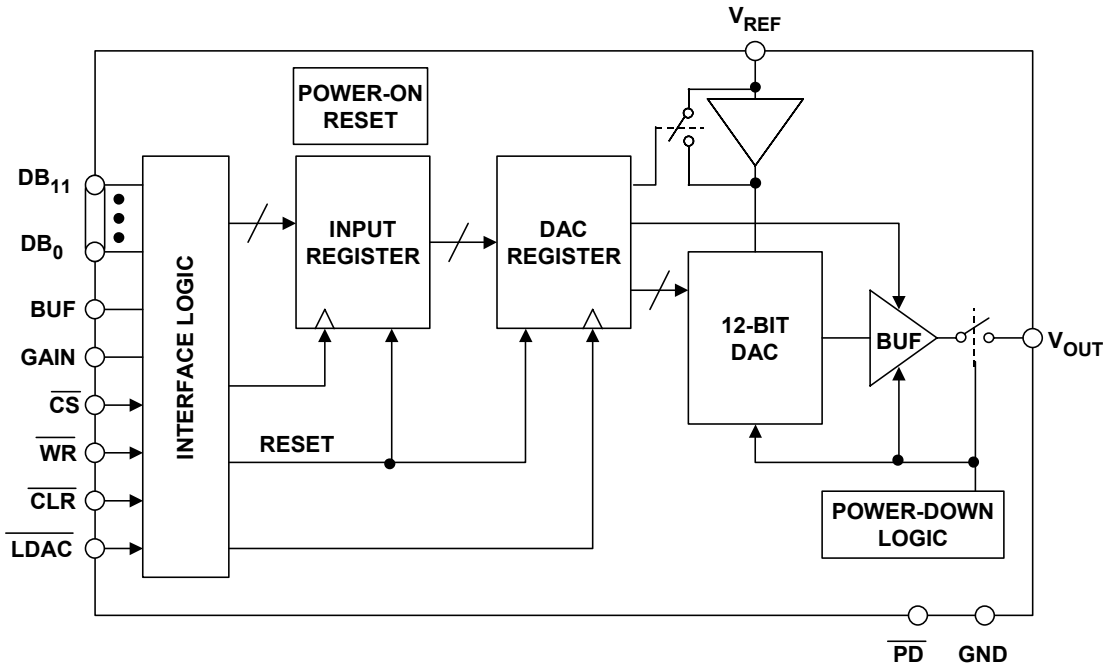



***Figure 6.64:*** *AD5340 12-Bit, 100-kSPS Parallel Input DAC*

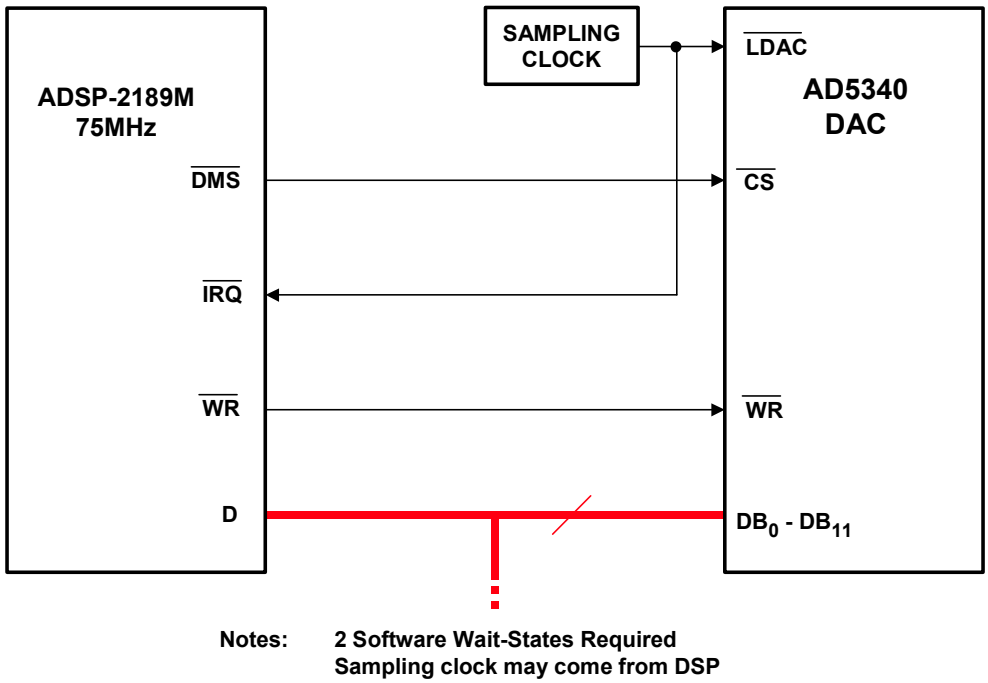



***Figure 6.65:*** *AD5340 DAC Parallel Interface to ADSP-2189M*

Finally, we will examine a high-speed TxDAC® parallel input DAC. The AD9726 is a 16-bit, 600-MSPS DAC that utilizes an LVDS interface to achieve the 600+ MSPS conversion rate (Reference 10). A simplified block diagram is shown in Figure 6.66.

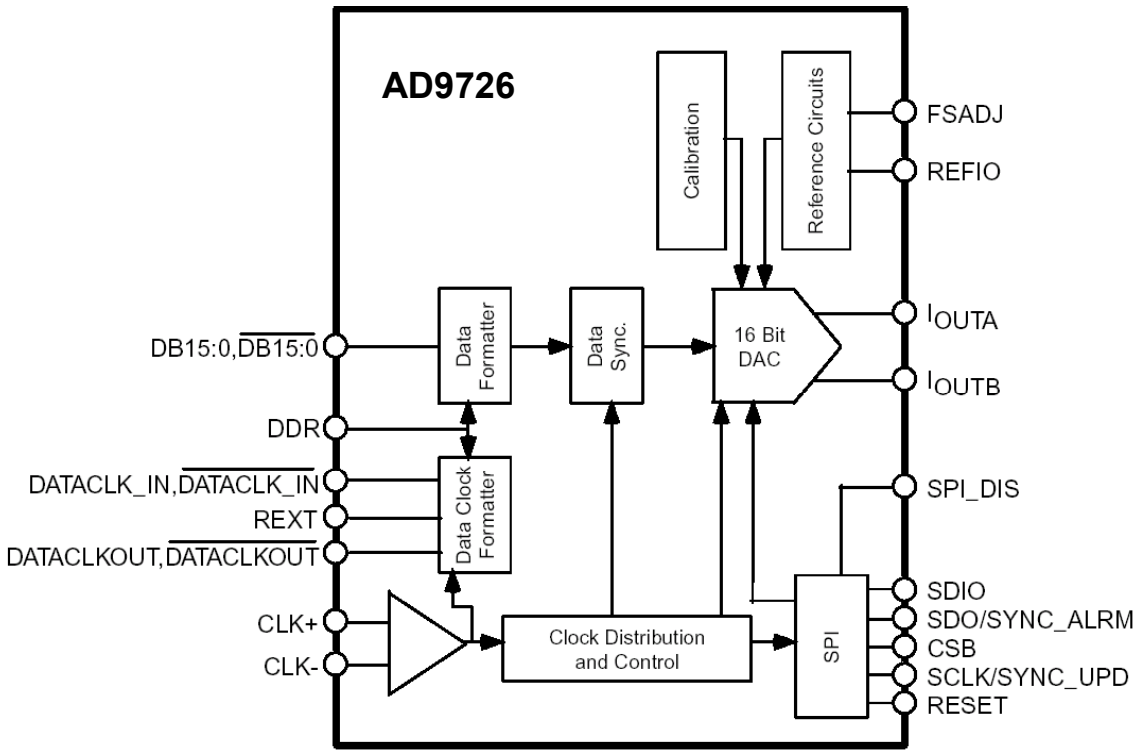



***Figure 6.66:*** *AD9726 16-Bit, 600+ MSPS DAC with LVDS Inputs*

In addition, this device also features unprecedented noise performance of –161 dBm/Hz for output frequencies between 100 MHz and 300 MHz and –169 dBm/Hz at 20-MHz output. This combination of high speed and low noise is ideal for maximizing signal synthesis performance in multicarrier communication systems, as well as in instrumentation and test applications.

# REFERENCES:
# 6.2 ADC AND DAC DIGITAL INTERFACES

1. Data sheet for AD7466/AD7467/AD7468 1.6-V, Micropower 12-/10-/8-Bit ADCs in 6-Lead SOT-23, http://www.analog.com.

2. Data sheet for AD9289 Quad 8-Bit, 65-MSPS Serial LVDS 3-V A/D Converter, http://www.analog.com.

3. Data sheet for AD7853/AD7853L 3-V to 5-V, Single-Supply, 200kSPS 12-Bit Sampling ADC, http://www.analog.com.

4. Data sheet for ADSP-2189M DSP Microcomputer, http://www.analog.com.

5. Walt Kester, **Mixed Signal and DSP Design Techniques**, Newnes, an Imprint of Elsevier Science, 2003, ISBN-0-75067-611-6, Section 8.

6. Data sheet for AD9430 12-Bit, 170-MSPS/210-MSPS 3.3-V A/D Converter, http://www.analog.com.

7. Data sheet for AD7854/AD7854L 3-V to 5-V Single-Supply, 200-kSPS 12-Bit Sampling ADC, http://www.analog.com.

8. Data sheet for AD5322 2.5-V to 5.5-V, 230 μA, Dual Rail-to-Rail Output DAC, http://www.analog.com.

9. Data sheet for AD5340 2.5-V to 5.5-V, 115 μA, Parallel Interface, Single Voltage Output DAC, http://www.analog.com.

10. Data sheet for AD9726 16-bit, 600+ MSPS LVDS Input D/A Converter, http://www.analog.com.

# NOTES:

# SECTION 6.3: BUFFERING DAC ANALOG OUTPUTS

*Walt Kester*

## Introduction

Modern IC DACs provide either voltage or current outputs. Figure 6.67 shows three fundamental configurations, all with the objective of using an op amp for a buffered and/or amplified output voltage.

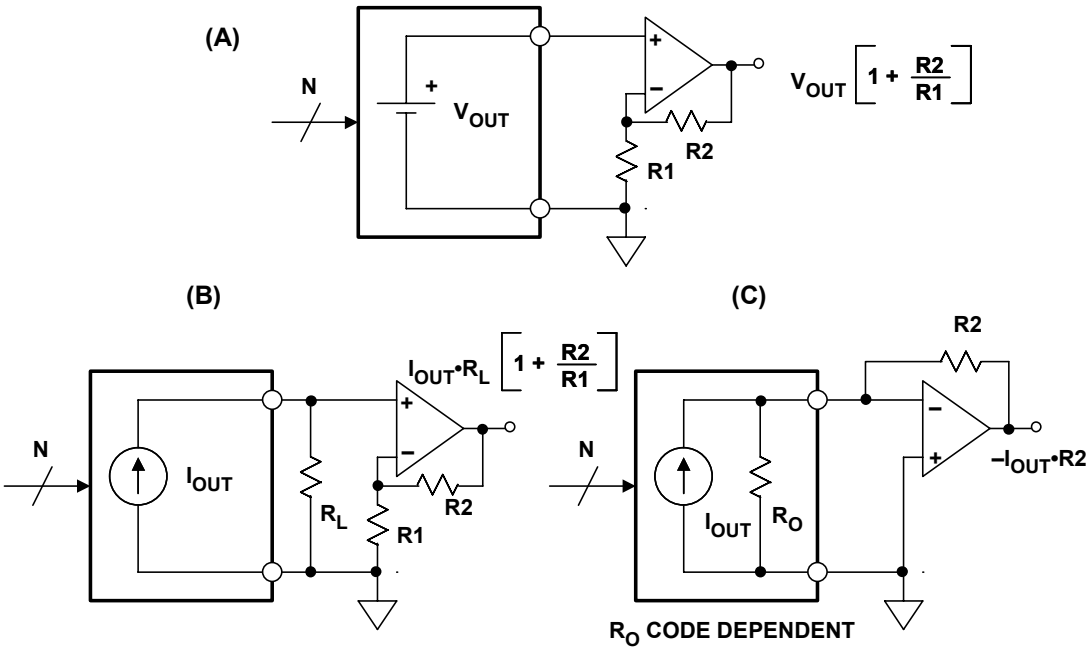



***Figure 6.67:*** *Buffering DAC Outputs with Op Amps*

Figure 6.67A shows a buffered voltage output DAC. In many cases, the DAC output can be used directly, without additional buffering. If an additional op amp buffer is needed, it is usually configured in a non-inverting mode, with gain determined by R1 and R2.

There are two basic methods for dealing with a current output DAC. In Figure 6.67B, a voltage is simply developed across external load resistor, $R_L$. An external op amp can be used to buffer and/or amplify this voltage if required. Many high speed DACs supply fullscale currents of 20 mA or more, thereby allowing reasonable voltages to be developed across fairly low value load resistors. For instance, fast settling video DACs typically supply nearly 30-mA fullscale current, allowing 1 V to be developed across a source and load terminated 75-Ω coaxial cable (representing a dc load of 37.5 Ω to the DAC output).

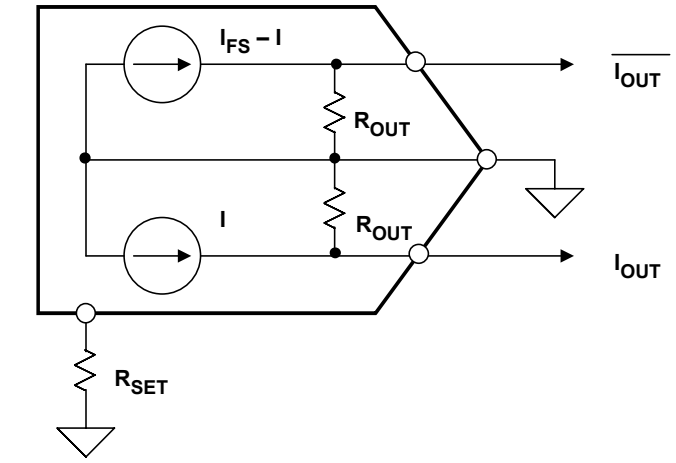
A direct method to convert the output current into a voltage is shown in Figure 6.67C. This circuit is usually called a current-to-voltage converter, or I/V. In this circuit, the DAC output drives the inverting input of an op amp, with the output voltage developed

across the R2 feedback resistor. In this approach the DAC output always operates at virtual ground (which may give a linearity improvement vis-à-vis Figure 6.67B). Note that an R-2R current-output CMOS DAC must use this configuration, because the output resistance, $R_O$, is dependent upon the output code (see Chapter 3 of this book on DAC architectures for more details).

The general selection process for an op amp used as a DAC buffer is similar to that of an ADC buffer. The same basic specifications such as dc accuracy, noise, settling time, bandwidth, distortion, etc., apply to DACs as well as ADCs, and the discussion will not be repeated here. Rather, some specific application examples will be shown.

## Differential to Single-Ended Conversion Techniques

A general model of a modern current output DAC is shown in Figure 6.68. This model is typical of the AD976x and AD977x TxDAC® series (see Reference 1). Current output is more popular than voltage output, especially at audio frequencies and above. If the DAC is fabricated on a bipolar or BiCMOS process, it is likely that the output will sink current, and that the output impedance will be less than 500 Ω (due to the internal R-2R resistive ladder network). On the other hand, a CMOS DAC is more likely to source output current and have a high output impedance, typically greater than 100 kΩ.




- **$I_{FS}$ 2 - 20mA typical**
- **Bipolar or BiCMOS DACs sink current, $R_{OUT}$ < 500Ω**
- **CMOS DACs source current, $R_{OUT}$ > 100kΩ**
- **Output compliance voltage < ±1V for best performance**

***Figure 6.68:*** *Generalized Model of a High Speed DAC Output such as the AD976x and AD977x Series*

Another consideration is the output *compliance voltage*—the maximum voltage swing allowed at the output in order for the DAC to maintain its linearity. This voltage is typically 1 V to 1.5 V, but can vary depending upon the DAC. Best DAC linearity is generally achieved when driving a virtual ground, such as an op amp I/V converter. However, better distortion performance is often achieved when the DAC is allowed to develop a small voltage across a resistive load.

Modern current output DACs usually have differential outputs, to achieve high common-mode rejection and reduce the even-order distortion products. Fullscale output currents in the range of 2 mA to 20 mA are common.

In many applications, it is desirable to convert the differential output of the DAC into a single-ended signal, suitable for driving a coax line. This can be readily achieved with an RF transformer, provided low frequency response is not required. Figure 6.69 shows a typical example of this approach. The high impedance current output of the DAC is terminated differentially with 50 Ω, which defines the source impedance to the transformer as 50 Ω.

The resulting differential voltage drives the primary of a 1:1 RF transformer, to develop a single-ended voltage at the output of the secondary winding. The output of the 50-Ω LC filter is matched with the 50-Ω load resistor $R_L$, and a final output voltage of 1-Vp-p is developed.

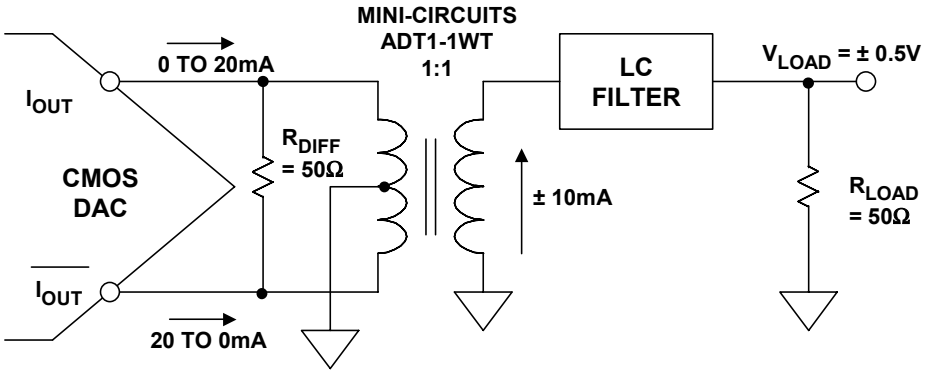



***Figure 6.69:*** *Differential Transformer Coupling*

The transformer not only serves to convert the differential output into a single-ended signal, but it also isolates the output of the DAC from the reactive load presented by the LC filter, thereby improving overall distortion performance.

An op amp connected as a differential to single-ended converter can be used to obtain a single-ended output when frequency response to dc is required. In Figure 6.70 the AD8055 op amp is used to achieve high bandwidth and low distortion (see Reference 2). The current output DAC drives balanced 25-Ω resistive loads, thereby developing an out-of-phase voltage of 0 to +0.5 V at each output.

The AD8055 is configured for a gain of 2, to develop a final single-ended ground-referenced output voltage of 2-V p-p. Note that because the output signal swings above and below ground, a dual-supply op amp is required.

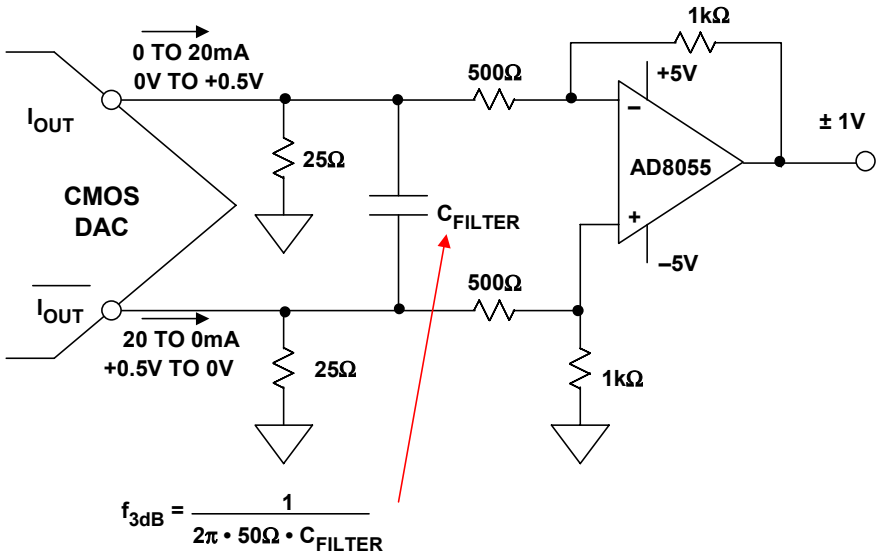



***Figure 6.70:*** *Differential DC Coupled Output Using a Dual Supply Op Amp*

The $C_{FILTER}$ capacitor forms a differential filter with the equivalent 50-Ω differential output impedance. This filter reduces any slew-induced distortion of the op amp, and the optimum cutoff frequency of the filter is determined empirically to give the best overall distortion performance.

A modified form of the Figure 6.70 circuit can be operated on a single supply, provided the common-mode voltage of the op amp is set to mid-supply (+2.5 V). This is shown in Figure 6.71, where the AD8061 op amp is used (Reference 3). The output voltage is 2-Vp-p centered around a common-mode voltage of +2.5 V. This common-mode voltage can be either developed from the +5-V supply using a resistor divider, or directly from a +2.5-V voltage reference. If the +5-V supply is used as the common-mode voltage, it must be heavily decoupled to prevent supply noise from being amplified.

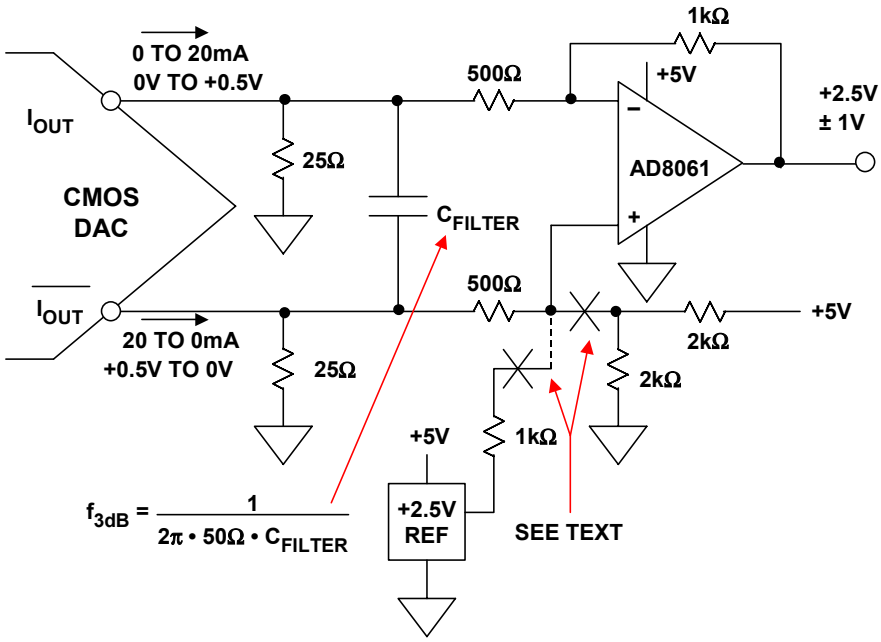



***Figure 6.71:*** *Differential DC Coupled Output Using a Single-Supply Op Amp*

## Single-Ended Current-to-Voltage Conversion

Single-ended current-to-voltage conversion is easily performed using a single op amp as an I/V converter, as shown in Figure 6.72. The 10-mA full scale DAC current from the AD768 (see Reference 4) develops a 0 to +2-V output voltage across the 200-Ω $R_F$ resistor.

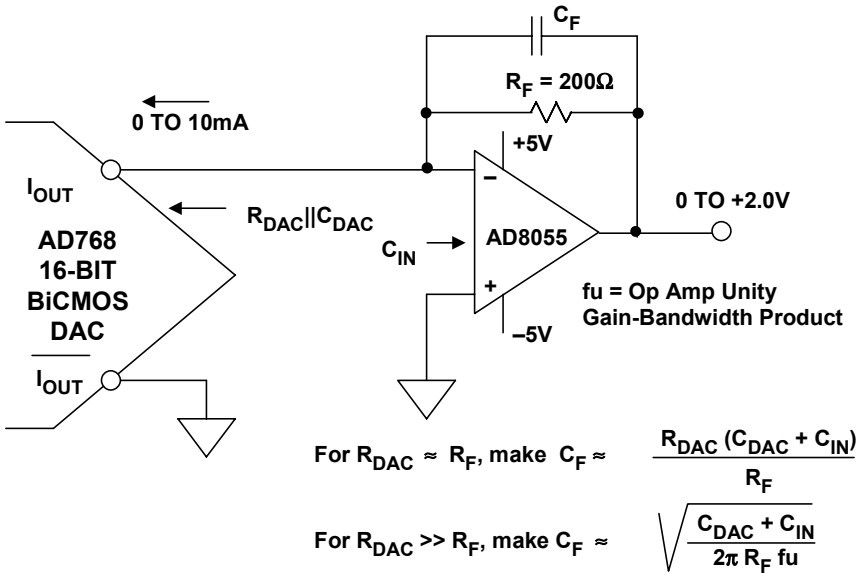



***Figure 6.72:*** *Single-Ended I/V Op Amp Interface for Precision 16-Bit AD768 DAC*

Driving the virtual ground of the AD8055 op amp minimizes any distortion due to nonlinearity in the DAC output impedance. In fact, most high resolution DACs of this type are factory trimmed using an I/V converter.

It should be recalled, however, that using the single-ended output of the DAC in this manner will cause degradation in the common-mode rejection and increased second-order distortion products, compared to a differential operating mode.

The $C_F$ feedback capacitor should be optimized for best pulse response in the circuit. The equations given in the diagram should only be used as guidelines. A much more detailed analysis of this type of circuit is given in Reference 6.

An R-2R based current-output DAC (see Chapter 3 of this book for details of the architecture) has a code-dependent output impedance—therefore, its output must drive the virtual ground of an op amp in order to maintain linearity. The AD5545/AD5555 16-/14-bit DAC is an excellent example of this architecture (Reference 6). A suitable interface circuit is shown in Figure 6.73 where the ADR03 is used as a 2.5-V voltage reference (Reference 7), and the AD8628 chopper-stabilized op amp (Reference 8) is used as an output I/V converter.

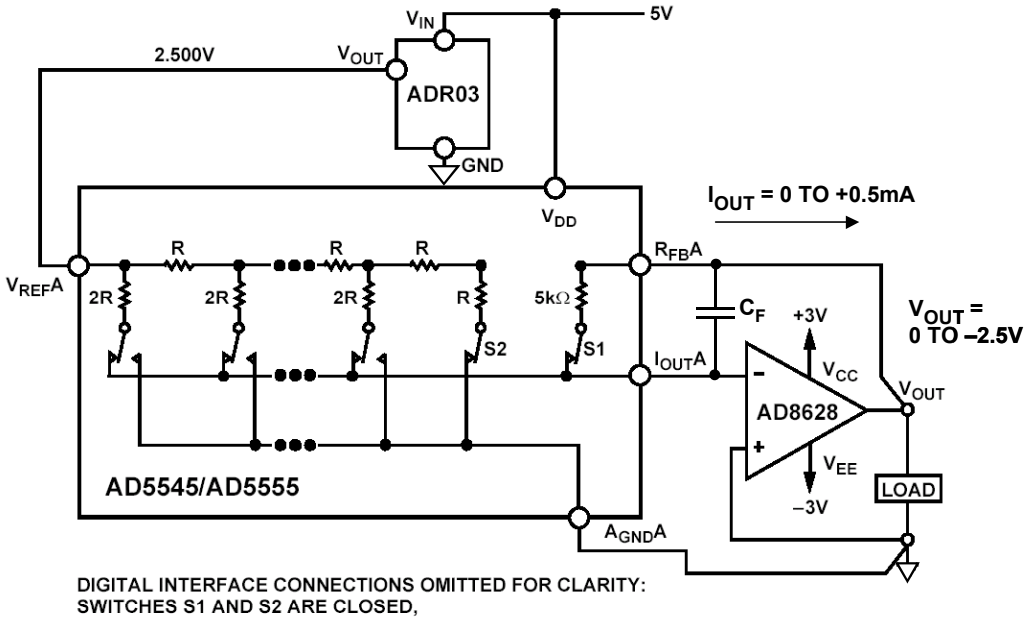



***Figure 6.73:*** *AD5545/AD5555 Dual 16-/14-Bit R-2R Current Output DAC Interface*

The external 2.5-V references determines the fullscale output current, 0.5 mA. Note that a 5-kΩ feedback resistor is included in the DAC, and using it will enhance temperature stability as opposed to using an external resistor. The fullscale output voltage from the op amp is therefore –2.5 V. The $C_F$ feedback capacitor compensates for the DAC output capacitance and should be selected to optimize the pulse response, with 20 pF a typical starting point.

## Differential Current-to-Differential Voltage Conversion

If a buffered differential voltage output is required from a current output DAC, the AD813x-series of differential amplifiers (Reference 9) can be used as shown in Figure 6.74.

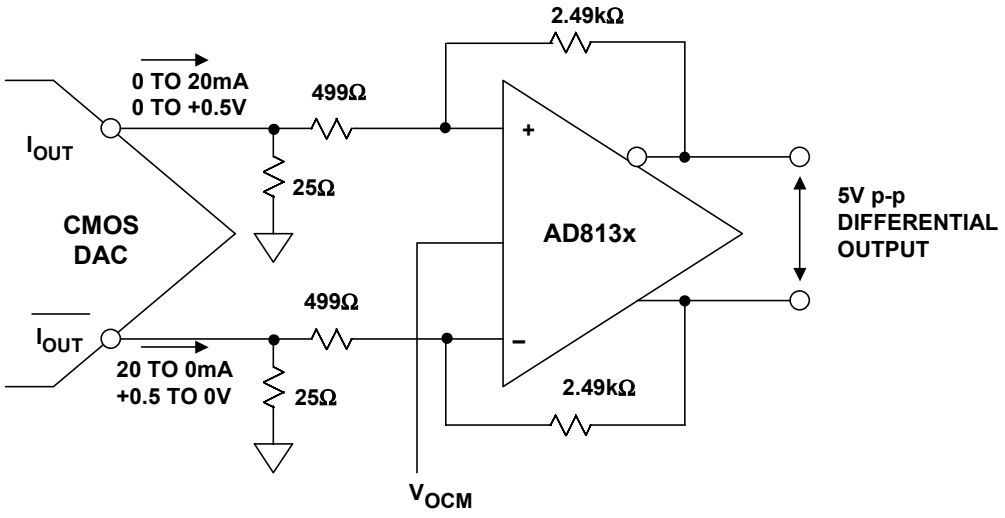



***Figure 6.74:*** *Buffering High Speed DACs Using AD813X Differential Amplifier*

The DAC output current is first converted into a voltage that is developed across the 25-Ω resistors. The voltage is amplified by a factor of 5 using the AD813x. This technique is used in lieu of a direct I/V conversion to prevent fast slewing DAC currents from overloading the amplifier and introducing distortion. Care must be taken so that the DAC output voltage is within its compliance rating.

The $V_{OCM}$ input on the AD813x can be used to set a final output common-mode voltage within the range of the AD813x. Adding a pair of 75-Ω series output resistors will allow transmission lines to be driven.

## An Active Lowpass Filter for Audio DAC

Figure 6.75 shows an active lowpass filter which also serves as a current-to-voltage converter for the AD1853 Σ-Δ audio DAC (see Reference 10). The filter is a 4-pole filter with a 3-dB cutoff frequency of approximately 75 kHz. Because of the high oversampling frequency (24.576 MSPS when operating the DAC at a 48-kSPS throughput rate), a simple filter is all that is required to remove aliased components above 12 MHz).

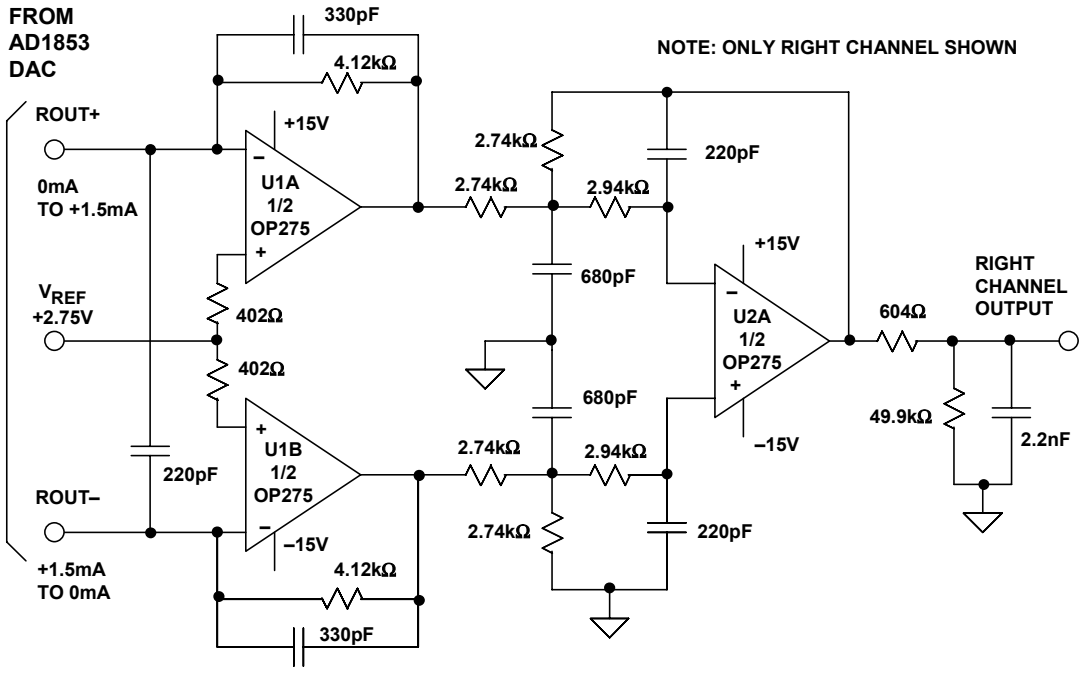



***Figure 6.75:*** *A 75-kHz 4-Pole Gaussian Active Filter for Buffering the Output of the AD1853 Stereo DAC*

The diagram shows a single channel for the dual channel DAC output. U1A and U1B I/V stages form a 1-pole differential filter, while U2 forms a 2-pole multiple-feedback filter that also performs a differential-to-single-ended conversion.

A final fourth passive pole is formed by the 604-Ω resistor and the 2.2-nF capacitor across the output. The OP275 op amp was chosen for operation as U1 and U2 because of its high quality audio characteristics (see Reference 11).

For further details of active filter designs, see Reference 12.

# REFERENCES:
# 6.3 BUFFERING DAC ANALOG OUTPUTS

1. Data sheet for AD9772A 14-Bit, 160 MSPS TxDAC+® with 2x Interpolation Filter**,** http://www.analog.com, for example. Also, see other members of the AD976x and AD977x family of communications DACs.

2. Data sheet for AD8055/AD8056 Low Cost, 300 MHz Voltage Feedback Amplifiers**,** http://www.analog.com.

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5. Walt Kester, **Practical Design Techniques for Sensor Signal Conditioning**, Analog Devices, 1999, ISBN-0-916550-20-6, Chapter 5, available for free download at http://www.analog.com.

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9. Data sheets for AD813x-Series Differential Amplifiers (AD8131, AD8132, AD8137, AD8138, AD8139), http://www.analog.com.

10. Data sheet for AD1853 Stereo, 24-Bit, 192 kHz, Multibit Σ-Δ DAC, http://www.analog.com.

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12. Walter G. Jung, **Op Amp Applications**, Analog Devices, 2002, ISBN 0-916550-26-5, Chapter 5.

# NOTES:

# SECTION 6.4: DATA CONVERTER VOLTAGE REFERENCES

*Walt Kester*

In most cases, the accuracy of a data converter is determined by a voltage reference of some sort. An exception to this, of course, is an ADC which operates in a *ratiometric* mode, where both the input signal and input range scale proportionally to the reference. In this specialized case, there is no requirement for an accurate reference, and the power supply is generally adequate. For details on ratiometric operation, see the discussion regarding the AD7730 Σ-Δ ADC in Chapter 3 of this book.

Some ADCs and DACs have internal references, while others do not. Some ADCs use the power supply as a reference. Unfortunately, there is little standardization with respect to ADC/DAC voltage references. In some cases, the dc accuracy of a converter with an internal reference can often be improved by overriding or replacing the internal reference with a more accurate and stable external one. In other cases, the use of an external low-noise reference will also increase the noise-free code resolution of a high-resolution ADC.

Various ADCs and DACs provide the capability to use external references in lieu of internal ones in various ways. Figure 6.76 shows some of the popular configurations (but certainly not all). Figure 6.76A shows a converter which requires an external reference. It is generally recommended that a suitable decoupling capacitor be added close to the ADC/DAC REF IN pin. The appropriate value is usually specified in the voltage reference data sheet. It is also important that the reference be stable with the required capacitive load (more on this to come).

Figure 6.76B shows a converter that has an internal reference, where the reference is also brought out to a pin on the device. This allows it to be used other places in the circuit, provided the loading does not exceed the rated value. Again, it is important to place the capacitor close to the converter pin. If the internal reference is pinned out for external use, its accuracy, stability, and temperature coefficient is usually specified on the ADC or DAC data sheet.

If the reference output is to be used other places in the circuit, the data sheet specifications regarding fanout and loading must be strictly observed. In addition, care must be taken in routing the reference output to minimize noise pickup. In many cases, a suitable op amp buffer should be used directly at the REF OUT pin before fanning out to various other parts of the circuit.

Figure 6.76C shows a converter which can use either the internal reference or an external one, but an extra package pin is required. If the internal reference is used, as in Figure 6.76C, REF OUT is simply externally connected to REF IN, and decoupled if required. If an external reference is used as shown n Figure 6.76D, REF OUT is left floating, and the external reference decoupled and applied to the REF IN pin. This arrangement is quite flexible for driving similar ADCs or DACs with the same reference in order to obtain good tracking between the devices.

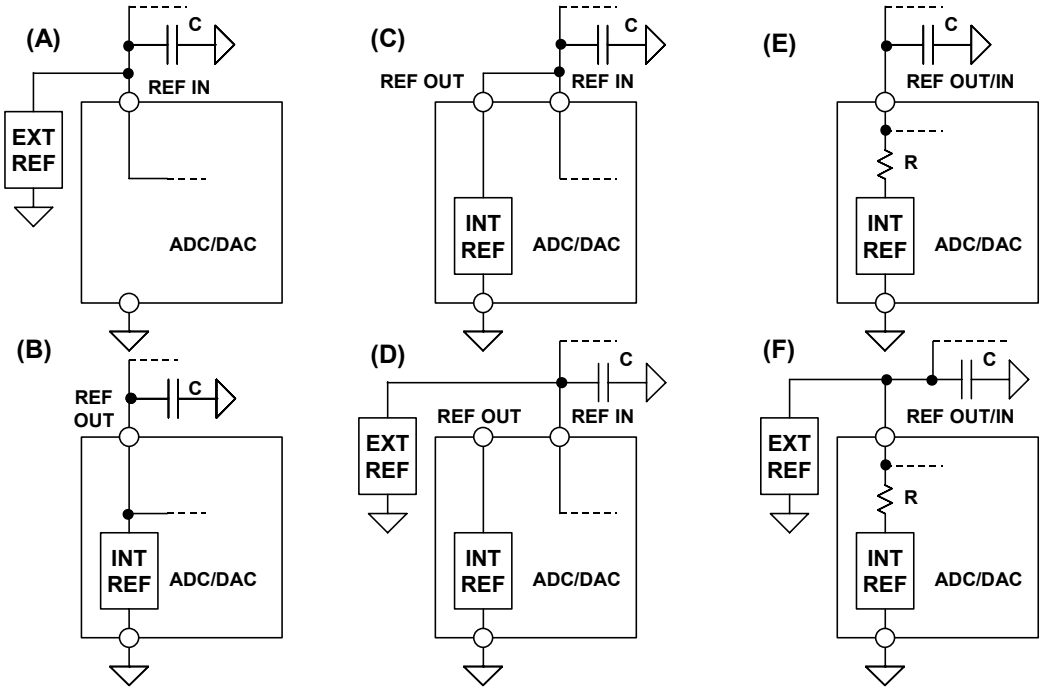


***Figure 6.76:*** *Some Popular ADC/DAC Reference Options*

Figure 6.76E shows an arrangement whereby an external reference can override the internal reference using a single package pin. The value of the resistor, R, is typically a few kΩ, thereby allowing the low impedance external reference to override the internal one when connected to the REF OUT/IN pin. Figure 6.76F shows how the external reference is connected to override the internal reference.

The arrangements shown in Figure 6.76 are by no means the only possible configurations for ADC and DAC references, and the individual data sheets should be consulted in all cases for details regarding options, fanout, decoupling, etc.

Although the reference element itself can be either a bandgap, buried zener, or XFET™ (see detailed discussion on voltage references in Chapter 7 of this book), practically all references have some type of output buffer op amp. The op amp isolates the reference element from the output and also provides drive capability. However, this op amp must obey the general laws relating to op amp stability, and that is what makes the topic of reference decoupling relevant to the discussion.

Note that a reference input to an ADC or DAC is similar to the analog input of an ADC, in that the internal conversion process can inject transient currents at that pin. This requires adequate decoupling to stabilize the reference voltage. Adding such decoupling might introduce instability in some reference types, depending on the output op amp design. Of course, a reference data sheet may not show any details of the output op amp, which leaves the designer in somewhat of a dilemma concerning whether or not it will be stable and free from transient errors. In many cases, the ADC or DAC data sheet will recommend appropriate external references and the recommended decoupling network.

Fortunately, some simple lab tests can exercise a reference circuit for transient errors, and also determine stability for capacitive loading (see Section 7.1 in Chapter 7 of this book for more details).

A well-designed voltage reference is stable with heavy capacitive decoupling. Unfortunately, some are not, and larger capacitors actually increases the amount of transient ringing. Such references are practically useless in data converter applications, because some amount of local decoupling is almost always required at the converter.

A suitable op amp buffer might be added between the reference and the data converter. But, there are many good references available (refer again to Section 7.1 of Chapter 7 in this book) which are stable with an output capacitor. This type of reference should be chosen for a data converter application, rather than incurring the further complication and expense of an op amp.

Figure 6.77 summarizes some important considerations for data converter references.

- **Data converter accuracy determined by the reference, whether internal or external, but ADC ratiometric operation can eliminate the need for accurate reference**
- **External references may offer better accuracy and lower noise than internal references**
- **Bandgap, buried zener, XFET® generally have on-chip output buffer op amp**
- **Transient loading can cause instability and errors**
- **External decoupling capacitors may cause oscillation**
- **Output may require external buffer to source and sink current**
- **Reference voltage noise may limit system resolution**

***Figure 6.77:*** *Data Converter Voltage Reference Considerations*

# NOTES:

# SECTION 6.5: SAMPLING CLOCK GENERATION

*Walt Kester*

## Introduction

In Chapter 2 of this book, we derived an extremely important relationship between broadband aperture jitter, $t_j$, converter SNR, and fullscale sinewave analog frequency, f:

$$SNR = 20\log_{10}\left[\frac{1}{2\pi f\, t_j}\right]. \qquad \text{Eq. 6.7}$$

This assumes an ideal ADC (or DAC), where the only error source is jitter. The bandwidth for the SNR measurement is the Nyquist bandwidth, dc to $f_s/2$, where $f_s$ is the sampling rate. Eq. 6.7 also assumes a fullscale sinewave input. The error due to jitter is proportional to the slew rate of the input signal—lower amplitude sinewaves with proportionally lower slew rate yield higher values of SNR (with respect to fullscale).

Another interesting case is the theoretical SNR due to jitter for non-sinusoidal signals, in particular those with a Gaussian frequency distribution. Because the average slew rate of this type of signal is less than a fullscale sinewave, the errors due to jitter are smaller. The mathematical treatment of this case is somewhat beyond the scope of the discussion, however.

It should be noted that $t_j$ in Eq. 6.7 is the combined jitter of the sampling clock, $t_{jc}$, and the ADC internal aperture jitter, $t_{ja}$—these terms are not correlated and therefore combine on an root-sum-square (rss) basis:

$$t_j = \sqrt{t_{jc}^{\,2} + t_{ja}^{\,2}}\,. \qquad \text{Eq. 6.8}$$

In many cases, the sampling clock jitter is several times larger than the ADC aperture jitter, and therefore is the dominate contributor to SNR degradation. For instance, the AD6645 14-bit, 80-/105-MSPS ADC has an rms aperture jitter specification of 0.1 ps. Meeting this jitter specification requires a low noise crystal oscillator.

While nothing can be done externally to change the ADC aperture jitter, there are a number things that can be done to ensure the sampling clock jitter is low enough so that the maximum possible performance is obtained from the ADC.

Figure 6.78 plots Eq. 6.7 and graphically illustrates how SNR is degraded by jitter for various fullscale analog input frequencies (note that we assume $t_j$ includes all jitter sources, including the internal ADC aperture jitter).

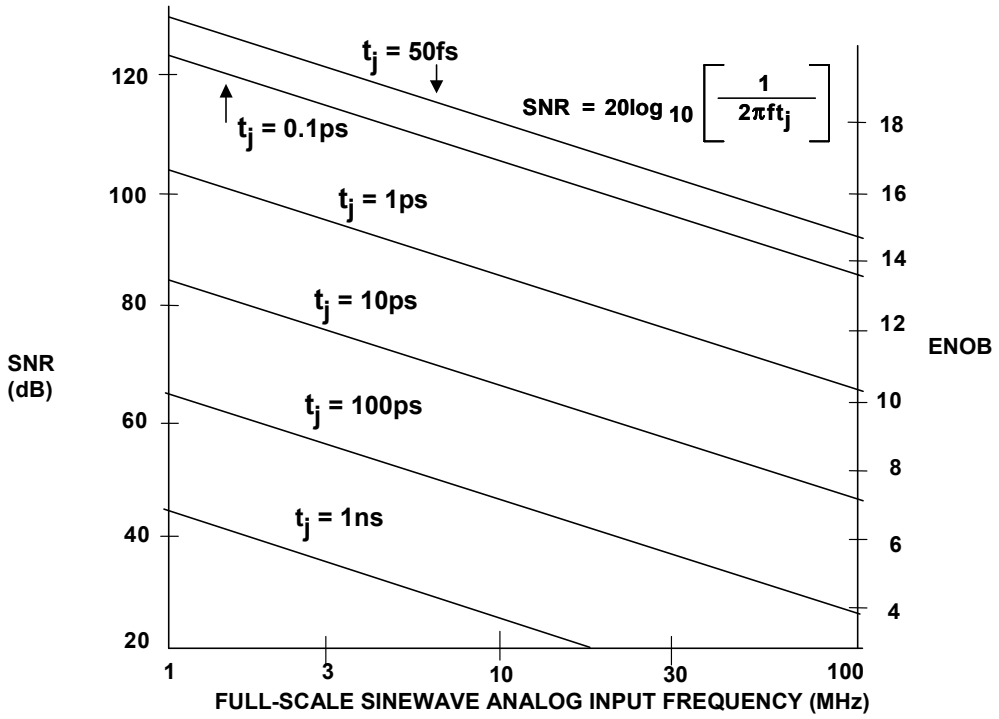


***Figure 6.78:*** *Theoretical SNR and ENOB Due to Jitter vs. Fullscale Sinewave Analog Input Frequency*

Recall from Chapter 2 of this book that there is a very useful relationship between effective number of bits (ENOB) and the signal-to-noise-plus-distortion ratio (SINAD) given by:

$$\text{ENOB} = \frac{\text{SINAD} - 1.76\ \text{dB}}{6.02\ \text{dB}}. \qquad \text{Eq. 6.8}$$

For the purposes of this discussion, assume that the ADC has no distortion, and therefore SINAD = SNR, so Eq. 6.8 becomes:

$$\text{ENOB} = \frac{\text{SNR} - 1.76\ \text{dB}}{6.02\ \text{dB}}. \qquad \text{Eq. 6.9}$$

The SNR values on the left-hand vertical axis of Figure 6.78 have been converted into ENOB values on the right-hand vertical axis using Eq. 6.9.

Figure 6.79 shows another plot of Eq. 6.7, where maximum allowable jitter, $t_j$, is plotted against fullscale analog input frequency for various values of ENOB. This plot is useful for determining the jitter requirements on the sampling clock (assuming that it dominates $t_j$) for various input frequencies and resolutions. For instance, digitization of a fullscale 30-MHz input requires less than 0.3-ps rms jitter to maintain 14-bit SNR performance.

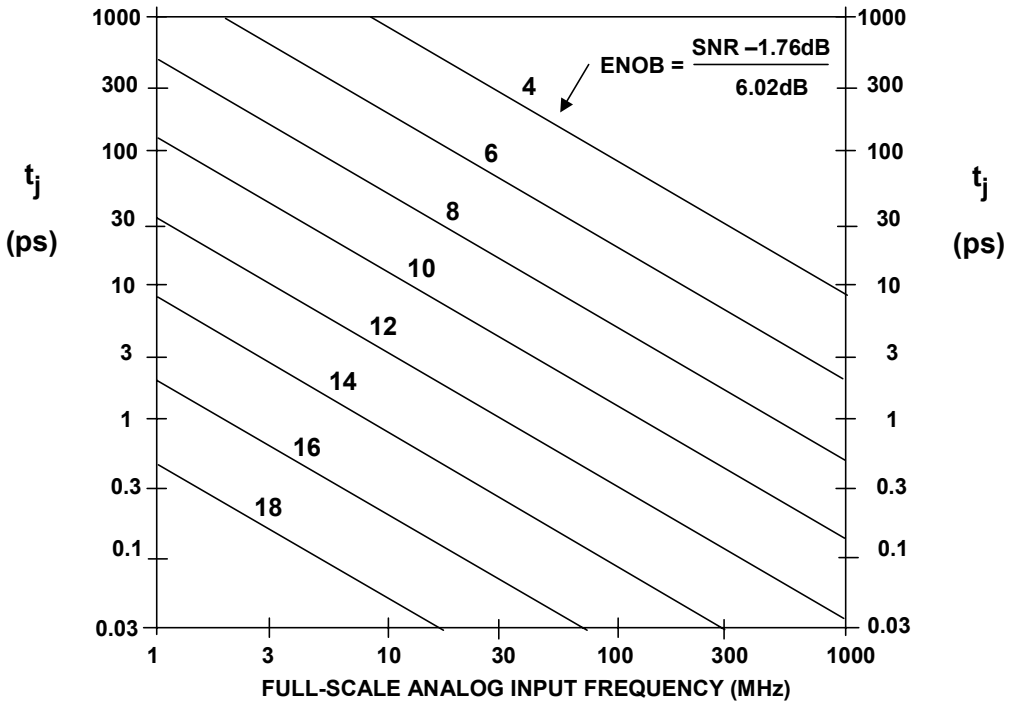


***Figure 6.79:*** *Maximum Allowable RMS Jitter vs. Fullscale Analog Input Frequency for Various Resolutions (ENOB)*

If the required sampling clock jitter is selected per the criteria set forth in Figure 6.79, then the SNR due to sampling clock jitter will equal the theoretical SNR of the ADC due to quantization noise.

In order to illustrate the significance of these jitter numbers, consider the typical rms jitter associated with a selection of logic gates shown in Figure 6.80. The values for the 74LS00, 74HCT00, and 74ACT00 were measured with a high performance ADC (aperture jitter less than 0.2-ps rms) using the method described in Chapter 5, where $t_j$ was calculated from FFT-based SNR degradation due to several identical gates connected in series. The jitter due to a single gate was then calculated by dividing by the square root of the total number of series-connected gates. The jitter for the MC100EL16 and NBSG16 was specified by the manufacturer.

- 74LS00 — 4.94 ps *
- 74HCT00 — 2.20 ps *
- 74ACT00 — 0.99 ps *
- MC100EL16 PECL — 0.7 ps **
- NBSG16, Reduced Swing ECL (0.4V) — 0.2 ps **

- * Calculated values based on degradation in ADC SNR
- ** Manufacturers' specification

***Figure 6.80:*** *RMS Jitter of Typical Logic Gates*

Further discussion on aperture jitter in sampled data systems can be found in References 1 and 2 and also in Chapter 2 of this book.

## Oscillator Phase Noise and Jitter

The previous analysis centered around broadband jitter, $t_j$. However, oscillators are most often specified in terms of phase noise. Therefore, the following discussion shows how to approximate the rms jitter based upon the phase noise.

First, a few definitions are in order. Figure 6.81 shows a typical output frequency spectrum of a non-ideal oscillator (i.e., one that has jitter in the time domain, corresponding to phase noise in the frequency domain). The spectrum shows the noise power in a 1-Hz bandwidth as a function of frequency. Phase noise is defined as the ratio of the noise in a 1-Hz bandwidth at a specified frequency offset, $f_m$, to the oscillator signal amplitude at frequency $f_O$.

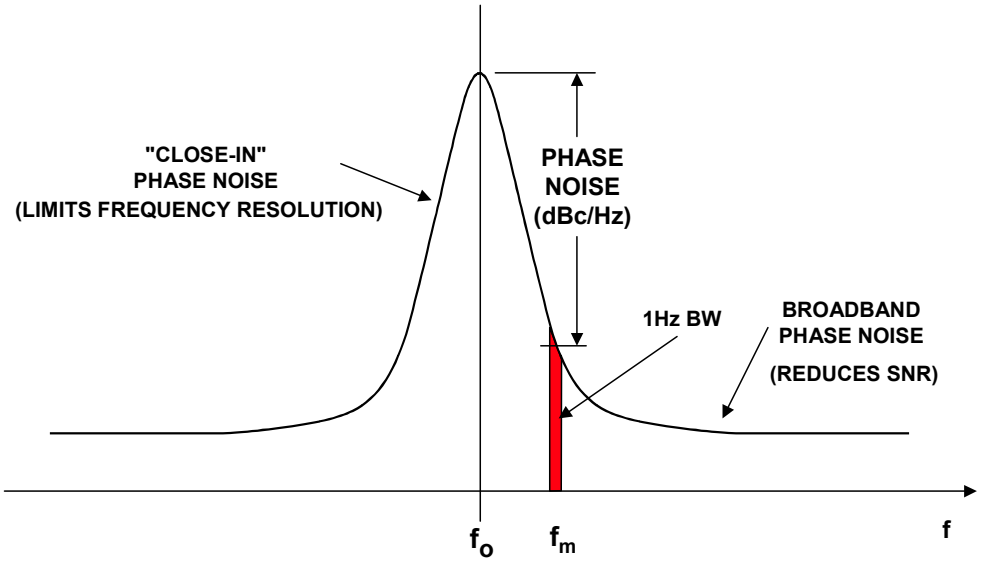


***Figure 6.81:*** *Oscillator Power Spectrum Due to Phase Noise*

The sampling process is basically a multiplication of the sampling clock and the analog input signal. This is multiplication in the time domain, which is equivalent to convolution in the frequency domain. Therefore, the spectrum of the sampling clock oscillator is convolved with the input and shows up on the FFT output of a pure sinewave input signal (see Figure 6.82). The "close-in" phase noise will "smear" the fundamental signal into a number of frequency bins, thereby reducing the overall spectral resolution. The "broadband" phase noise will cause a degradation in the overall SNR as predicted approximately by Eq. 6.7.

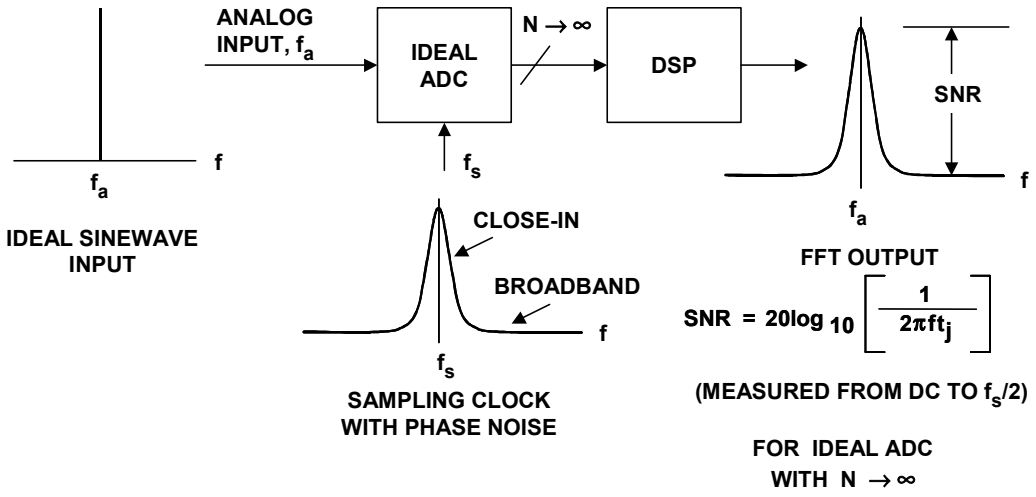


***Figure 6.82:*** *Effect of Sampling Clock Phase Noise Ideal Digitized Sinewave*

It is customary to characterize an oscillator in terms of its single-sideband phase noise as shown in Figure 6.83, where the phase noise in dBc/Hz is plotted as a function of frequency offset, $f_m$, with the frequency axis on a log scale. Note the actual curve is approximated by a number of regions, each having a slope of $1/f^x$, where x = 0 corresponds to the "white" phase noise region (slope = 0 dB/decade), and x = 1 corresponds to the "flicker" phase noise region (slope = –20 dB/decade). There are also regions where x = 2, 3, 4, and these regions occur progressively closer to the carrier frequency.

Note that the phase noise curve is somewhat analogous to the input voltage noise spectral density of an amplifier. Like amplifier voltage noise, low 1/f corner frequencies are highly desirable in an oscillator.

We have seen that oscillators are typically specified in terms of phase noise, but in order to relate phase noise to ADC performance, the phase noise must be converted into jitter. In order to make the graph relevant to modern ADC applications, the oscillator frequency (sampling frequency) is chosen to be 100 MHz for discussion purposes, and a typical graph is shown in Figure 6.84. Notice that the phase noise curve is approximated by a number of individual line segments, and the end points of each segment are defined by data points.

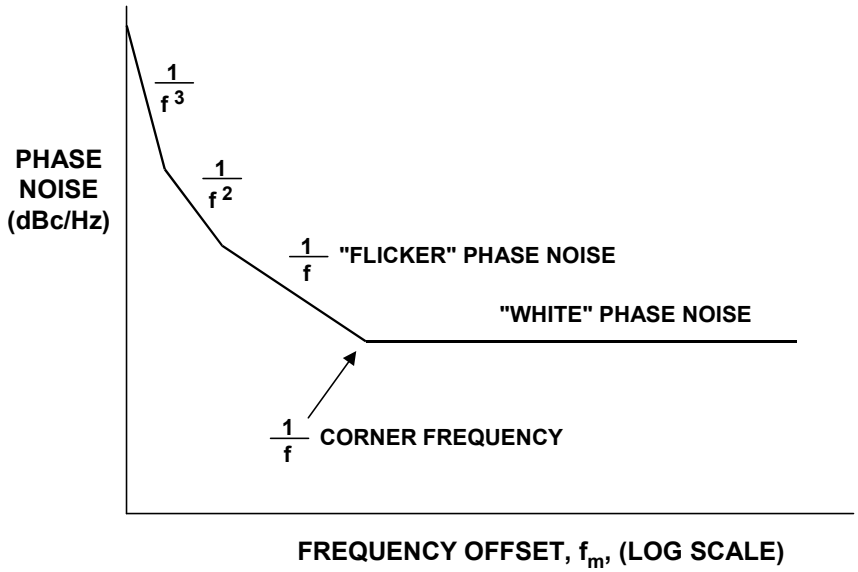


***Figure 6.83:*** *Oscillator Phase Noise in dBc/Hz vs. Frequency Offset*

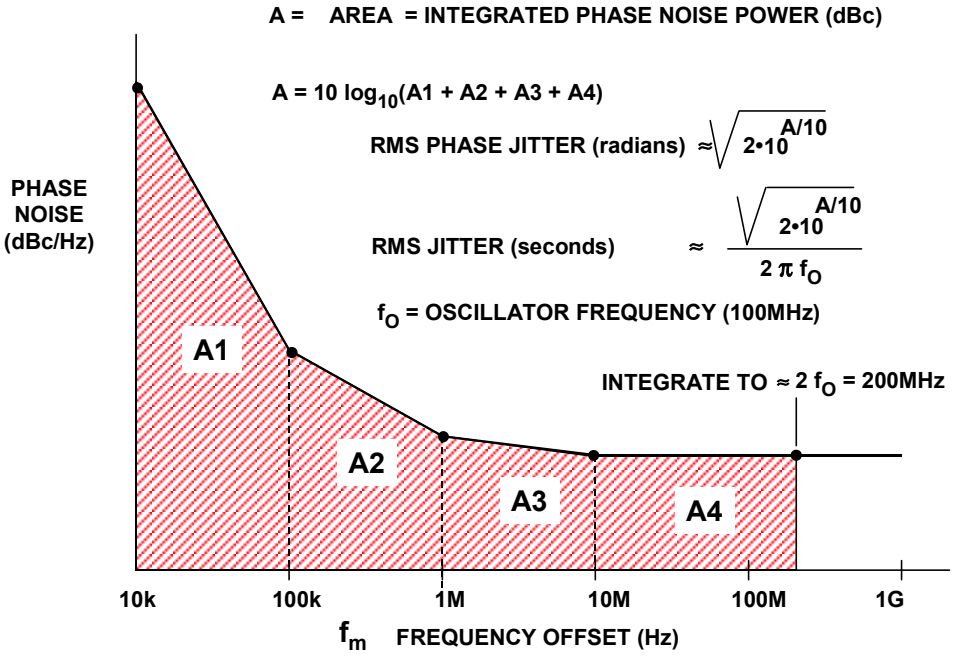


***Figure 6.84:*** *Calculating Jitter from Phase Noise*

The first step in calculating the equivalent rms jitter is to obtain the integrated phase noise power over the frequency range of interest, i.e., the area of the curve, A. The curve is broken into a number of individual areas (A1, A2, A3, A4), each defined by two data points. Generally speaking, the upper frequency range for the integration should be twice the sampling frequency, assuming there is no filtering between the oscillator and the ADC input. This approximates the bandwidth of the ADC sampling clock input.

Selecting the lower frequency for the integration also requires some judgment. In theory, it should be as low as possible to get the true rms jitter. In practice, however, the oscillator specifications generally will not be given for offset frequencies less than 10 Hz, or so—however, this will certainly give accurate enough results in the calculations. A lower frequency of integration of 100 Hz is also reasonable in most cases, if that specification is available. Otherwise, use either the 1-kHz or 10-kHz data point.

One should also consider that the "close-in" phase noise affects the spectral resolution of the system, while the broadband noise affects the overall system SNR. Probably the wisest approach is to integrate each area separately as explained below and examine the magnitude of the jitter contribution of each area. The low frequency contributions may be negligible compared to the broadband contribution if a crystal oscillator is used. Other types of oscillators may have significant jitter contributions in the low frequency area, and a decision must be made regarding their importance to the overall system frequency resolution.

The integration of each individual area yields individual power ratios. The individual areas are then summed and converted back into dBc. Once the integrated phase noise power is known, the rms phase jitter in radians is given by the equation (see References 3-7 for further details, derivations, etc.),

$$\text{RMS Phase Jitter (radians)} = \sqrt{2 \cdot 10^{A/10}}\ , \qquad \text{Eq. 6.10}$$

and dividing by $2\pi f_O$ converts the jitter in radians to jitter in seconds:

$$\text{RMS Phase Jitter (seconds)} = \frac{\sqrt{2 \cdot 10^{A/10}}}{2\pi\ f_O}\ . \qquad \text{Eq. 6.11}$$

It should be noted that computer programs and spreadsheets are available online to perform the integration by segments and calculate the rms jitter, thereby greatly simplifying the process (References 8, 9).

Figure 6.85 shows a sample calculation which assumes only broadband phase noise. The broadband phase noise chosen of –150 dBc/Hz represents a reasonably good signal generator specification, so the jitter number obtained represents a practical situation. The phase noise of –150 dBc/Hz (expressed as a ratio) is multiplied by the bandwidth of integration (200 MHz) to obtain the integrated phase noise of –67 dBc. Note that this multiplication is equivalent to adding the quantity $10 \log_{10}$[200 MHz – 0.01 MHz] to the phase noise in dBc/Hz. In practice, the lower frequency limit of 0.01 MHz can be dropped from the calculation, as it does not affect the final result significantly. A total rms jitter of approximately 1 ps is obtained using Eq. 6.11.

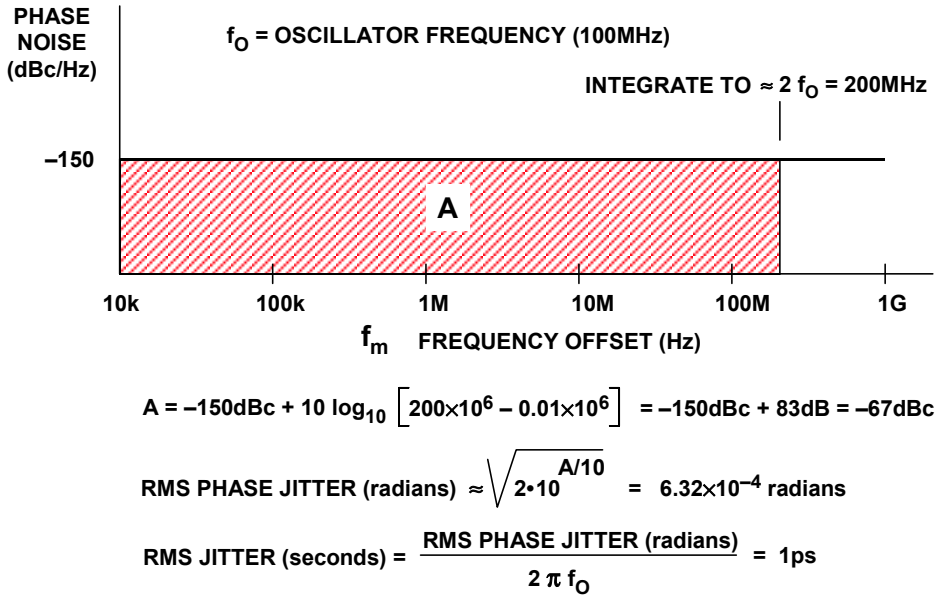


***Figure 6.85:*** *Sample Jitter Calculation Assuming Broadband Phase Noise*

Crystal oscillators generally offer the lowest possible phase noise and jitter, and some examples are shown for comparison in Figure 6.86. All the oscillators shown have a typical 1/f corner frequency of 20 kHz, and the phase noise therefore represents the white phase noise level. The two Wenzel oscillators are fixed-frequency and represent excellent performance (Reference 9). It is difficult to achieve this level of performance with variable frequency signal generators, as shown by the –150 dBc specification for a relatively high quality generator.

- **Wenzel ULN Series*** **–174dBc/Hz @ 10kHz+, ~ $1,500**
- **Wenzel Sprinter Series,** **–165dBc/Hz @ 10kHz+, ~ $350**
- **High Quality Signal Generator** **–150dBc/Hz @ 10kHz+, ~ $10,000**

  - **Thermal noise floor of resistive source in a matched system @ +25°C = –174dBm/Hz**
  - **0dBm = 1mW = 632mV p-p into 50Ω**
  - *** An oscillator with an output of +13dBm (2.82V p-p) into 50Ω with a phase noise of –174dBc/Hz has a noise floor of +13dBm – 174dBc = –161dBm, 13dB above the thermal noise floor**

**(Wenzel ULN and Sprinter Series Specifications and Pricing Used with Permission of Wenzel Associates)**

***Figure 6.86:*** *100-MHz Oscillator Broadband Phase Noise Floor Comparisons (Wenzel ULN and Sprinter Series Specifications and Pricing used with Permission of Wenzel Associates)*

At this point, it should be noted that there is a theoretical limit to the noise floor of an oscillator determined by the thermal noise of a matched source: –174 dBm/Hz at +25°C. Therefore, an oscillator with a +13-dBm output into 50 Ω (2.82-V p-p) with a phase noise of –174 dBc/Hz has a noise floor of –174 dBc + 13 dBm = –161 dBm. This is the case for the Wenzel ULN series as shown in Figure 6.87.

Figure 6.87 shows the jitter calculations from the two Wenzel crystal oscillators. In each case, the data points were taken directly for the manufacturer's data sheet. Because of the low 1/f corner frequency, the majority of the jitter is due to the "white" phase noise area. The calculated values of 63 femtoseconds (ULN-Series) and 180 femtoseconds represent extremely low jitter. For informational purposes, the individual jitter contributions of each area have been labeled separately. The total jitter is the root-sum-square of the individual jitter contributors.

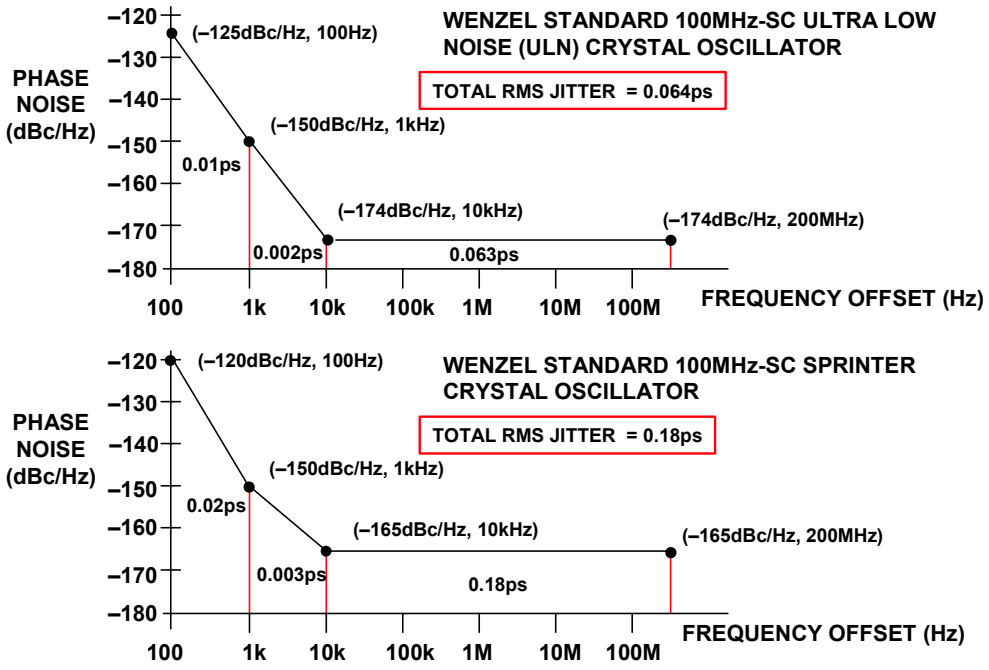


***Figure 6.87:*** *Jitter Calculations for Low Noise 100-MHz Crystal Oscillators (Phase Noise Data used with Permission of Wenzel Associates)*

In system designs requiring low jitter sampling clocks, the costs of low noise dedicated crystal oscillators is generally prohibitive. An alternative solution is to use a phase-locked-loop (PLL) in conjunction with a voltage-controlled oscillator to "clean up" a noisy system clock as shown in Figure 6.88. There are many good references on PLL design (see References 10-13, for example), and we will not pursue that topic further, other than to state that using a narrow bandwidth loop filter in conjunction with a voltage-controlled crystal oscillator (VCXO) typically gives the lowest phase noise. As shown in Figure 6.88, the PLL tends to reduce the "close-in" phase noise while at the same time, reducing the overall phase noise floor. Further reduction in the white noise floor can be obtained by following the PLL output with an appropriate bandpass filter.

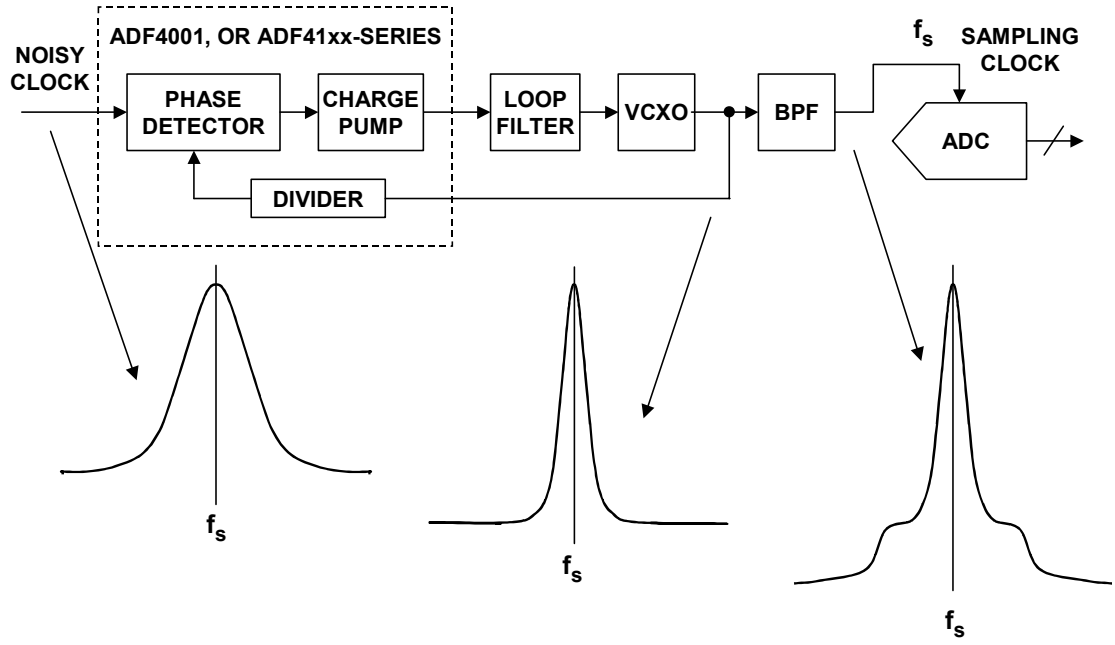


***Figure 6.88:*** *Using a Phase-Locked Loop (PLL) and Bandpass Filter to Condition a Noisy Clock Source*

The effect of enclosing a free-running VCO within a PLL is shown in Figure 6.89. Notice that the "close-in" phase noise is reduced significantly by the action of the PLL.

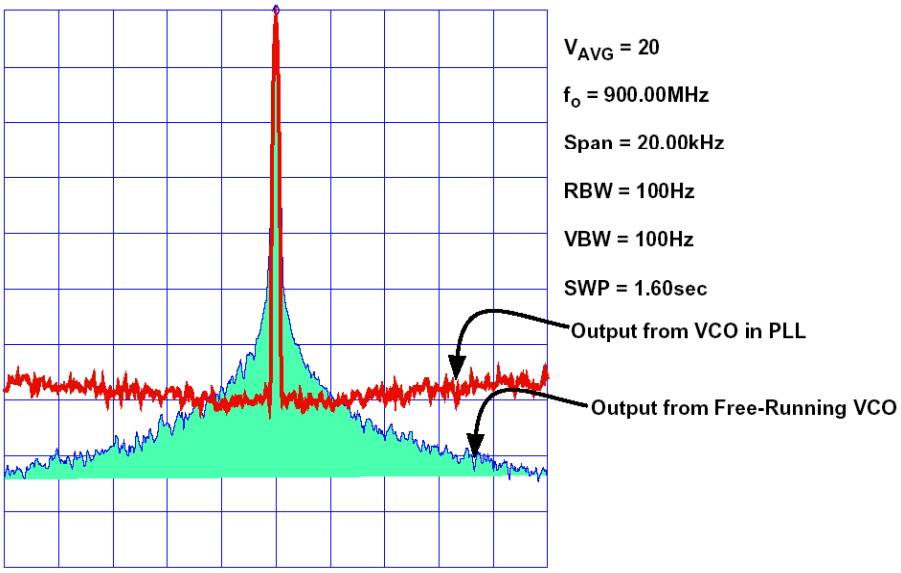


***Figure 6.89:*** *Phase Noise for a Free-Running VCO and a PLL-Connected VCO*

Analog Devices offers a wide portfolio of frequency synthesis products, including DDS systems, N, and fractional-N PLLs. For example, the ADF4360 is a fully integrated PLL complete with an internal VCO. With a 10-kHz bandwidth loop filter, the phase noise is shown in Figure 6.90, along with the line-segment approximation and jitter calculations in Figure 6.90. Note that the rms jitter is only 1.57 ps, even with a non-crystal VCO.

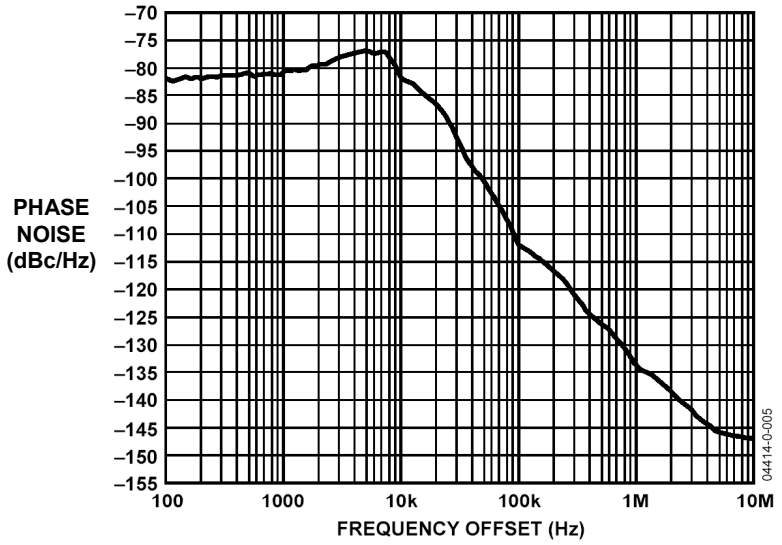


***Figure 6.90:*** *Phase Noise for ADF4360 2.25-GHz PLL with Loop Filter BW = 10 kHz*

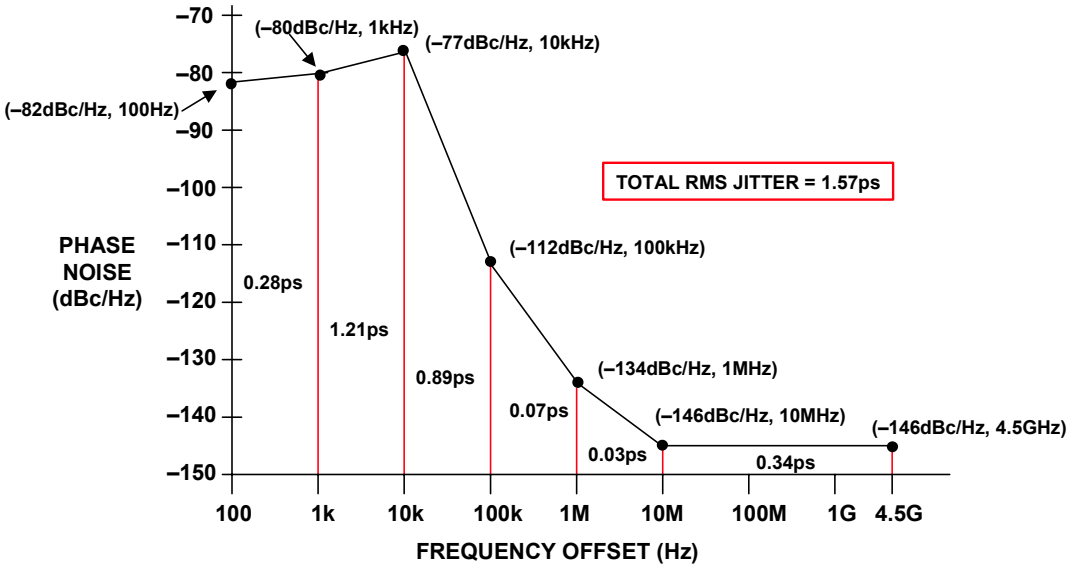


***Figure 6.91:*** *Line Segment Approximation to ADF4360 2.25GHz PLL Phase Noise Showing Jitter*

Historically, PLL design relied heavily on textbooks and application notes to assist in the design of the loop filter, etc. Now, with Analog Devices free downloadable ADIsimPLL software, PLL design is much easier. To start, choose a circuit by entering the desired output frequency range, and select a PLL, VCO, and a crystal reference. Once the loop filter configuration has been selected, the circuit can be analyzed and optimized for phase noise, phase margin, gain, spur levels, lock time, etc., in both the frequency and time domain. The program also performs the rms jitter calculation based on the PLL phase noise, thereby allowing the evaluation of the final PLL output as a sampling clock.

Figure 6.92 summarizes this discussion and should serve as an approximate guideline for selecting the type of sampling clock generator based upon the maximum input frequency and the required resolution in ENOB. The PLL approach with a standard VCO is an excellent one for generating sampling clocks where the rms jitter requirement is approximately 1 ps or greater. However, sub-picosecond jitter requires either a VCXO-based PLL or a dedicated low noise crystal oscillator.

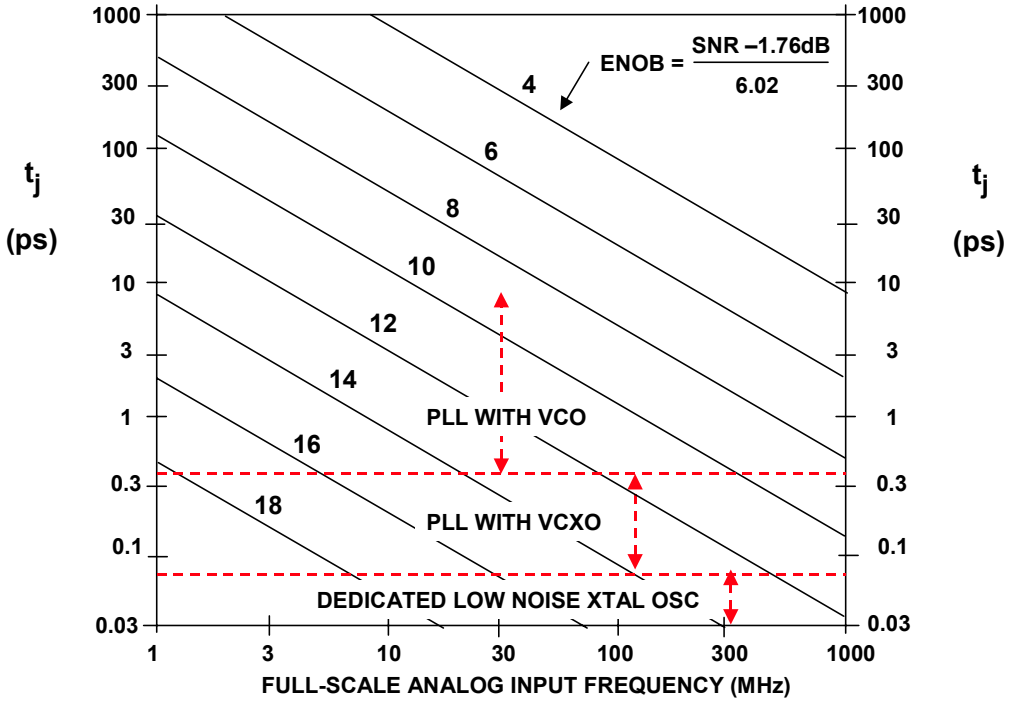


***Figure 6.92:*** *Oscillator Requirements vs. Resolution and Analog Input Frequency*

## "Hybrid" Clock Generators

DDSs, mixers, frequency dividers, and frequency doublers can be utilized in conjunction with PLLs to form what is generally referred to as a "hybrid" frequency synthesizer. An excellent tutorial on the subject can be found in Reference 14. A very simple example is shown in Figure 6.93 where a DDS system drives a PLL. The upper output frequency of the DDS system is of course limited by its maximum update rate. The upper frequency of a PLL, on the other hand, is primarily limited by the VCO, which can operate in the GHz range if required.

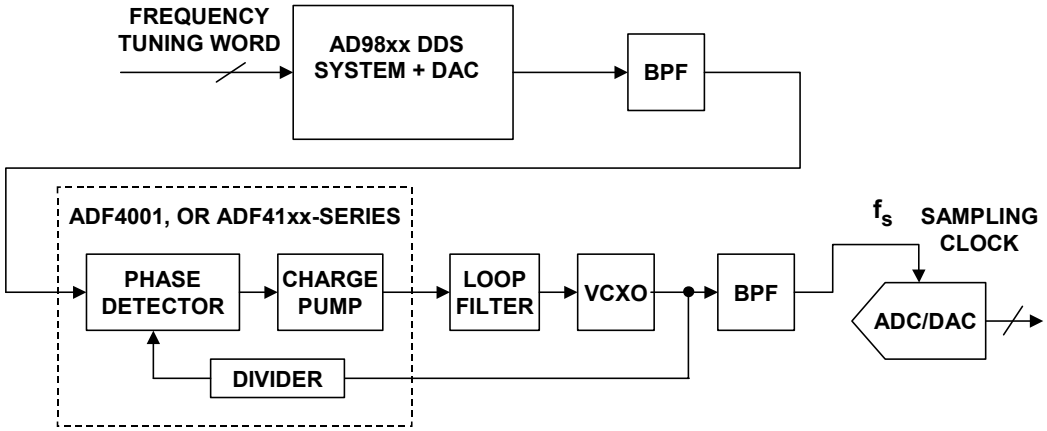


***Figure 6.93:*** *A Simple "Hybrid" Sampling Clock Generator*

As previously discussed, the phase noise of a PLL can be controlled by the loop filter, the VCXO, and an output filter. DDS systems have phase noise which is produced primarily by the finite resolution of the internal DAC. The system of Figure 6.93 uses the PLL to "clean up" the phase noise produced by the DDS system, thereby generating an output clock which is suitable for high performance ADC/DAC sampling clocks. There are many possible combinations possible if one looks at some of the configurations suggested in Reference 14.

In many less-demanding applications, DDS outputs can of course be used directly as a clock generator. Many DDSs have on-chip comparators which facilitate the generation of a square wave output.

Regardless of how it is generated, the overriding requirements on the sampling clock are ultimately dictated by the principles set forth in this section which relate phase noise and timing jitter to SNR.

## Driving Differential Sampling Clock Inputs

Data converters which can tolerate sampling clocks with tens of picoseconds or more of jitter can be driven from most any single-ended logic gate. However, for jitter requirements of 10 ps or less, more care must be taken in the selection of an appropriate driver. High performance high-speed data converters are almost always designed to accept a differential sampling clock input as shown in Figure 6.94.

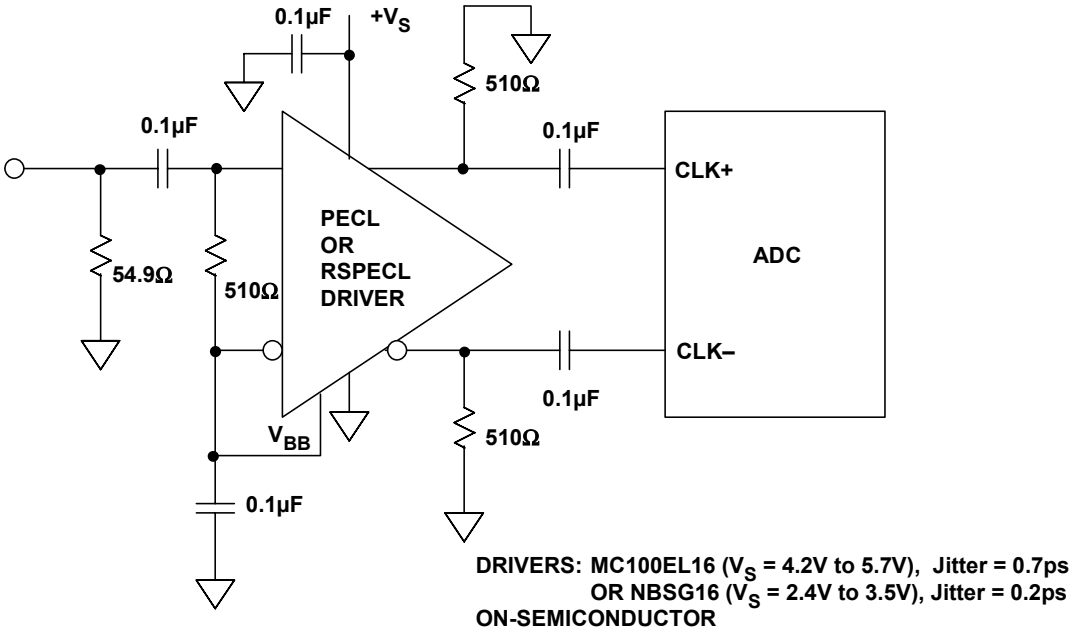


***Figure 6.94:*** *Low Jitter Single-Ended to Differential Clock Drivers*

Differential sampling clock inputs are popular with high speed converters and provide good common-mode rejection, thereby minimizing the possibility of corruption. It is also generally recommended that differential inputs be driven with low-level signals such as ECL (emitter-coupled logc), RSECL (reduced signal ECL), or LVDS (low voltage differential signal). A sampling clock that has a full swing between ground and the supply voltage will generally introduce extra noise, thereby degrading the overall converter dynamic performance. A high performance ADC data sheet should provide appropriate guidance for the optimum drive level.

Most oscillator or PLL outputs are single-ended, so a low-jitter PECL receiver/driver such as the ON-Semiconductor MC100EL16 or the NBSG16 (Reference 14) are excellent choices for performing single-ended to differential clock conversion. The rms jitter specification is 0.7 ps for the MC100EL16, and 0.2 ps for the NBSG16 (a silicon-germanium device). These parts are basically ECL (Emitter-Coupled-Logic) designs which can be operated on a single positive supply—hence the acronym "PECL" (Positive Emitter Coupled Logic). In almost all cases, the differential sampling clock inputs of the ADC are internally biased at the appropriate dc common-mode level, and the differential driver outputs can simply be ac-coupled to the ADC clock inputs. If the ADC does not have internal biasing, then an external resistor network is required to supply the required bias voltages.

The output voltage swing for the MC100EL16 PECL device is approximately 1-V p-p single-ended (2-V p-p differential), and 0.4-V p-p single-ended (0.8-V p-p differential) for the reduced-swing PECL (RSPECL) NBSG16.

For the ultra low-jitter applications, an RF transformer should be used to convert the single-ended oscillator output into a differential signal as shown in Figure 6.95. The back-to-back Schottky diodes limit the differential voltage input swing to about 0.8 V,

the 0.1-µF prevents any dc components from causing transformer saturation, and the 100-Ω resistor limits the output current of the drive oscillator. The AD6645 14-bit, 105-MSPS ADC has an aperture jitter specification of 0.1 ps, and the transformer drive circuit in conjunction with a very low noise oscillator will provide optimum performance with this type of low-jitter ADC. Some experimentation may be required to determine the amplitude for the input sinewave which gives the best overall SNR.

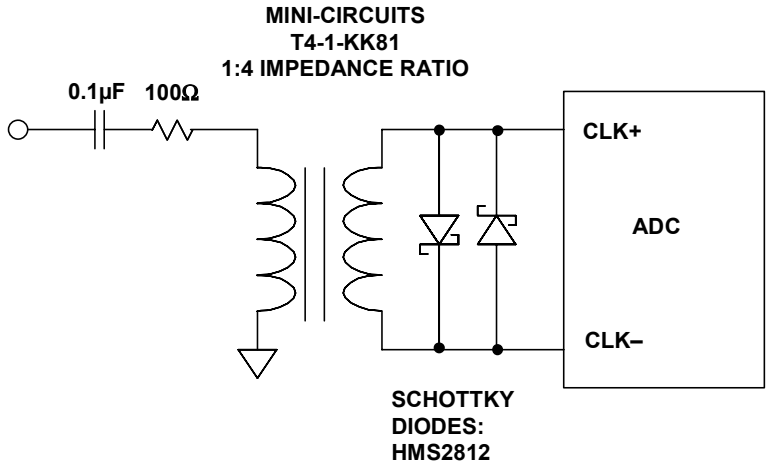


***Figure 6.95:*** *Single-Ended to Differential Conversion Using RF Transformer*

As in the case of ADC analog inputs and DAC analog outputs, there are other possibilities, and the device data sheet must always be consulted for the optimum sampling clock drive recommendations.

## Sampling Clock Summary

Earlier in this chapter, we discussed the importance of the drive circuitry for the analog input of an ADC and the analog output buffer for a DAC. Equally important is the ADC or DAC sampling clock. Regarding the sampling clock as simply another "digital" signal is a certain receipt for disaster in a system design.

This section has described the effects of jitter on SNR, assuming that the jitter is solely a combination of the internal ADC aperture jitter and the external sampling clock jitter. However, improper layout, grounding, and decoupling techniques can create additional clock jitter which can drastically degrade dynamic performance, regardless of the specifications of the ADC or sampling clock oscillator.

Routing the sampling clock signal in parallel with noisy digital signals is sure to degrade performance due to stray coupling. In fact, coupling high speed data from parallel output ADCs into the sampling clock not only increases noise, but is likely to create additional harmonic distortion, because the energy contained in the digital output transient currents is signal dependent. For further discussion of these and other critical hardware design techniques, the reader is referred to Chapter 9 of this book.

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# 6.5 SAMPLING CLOCK GENERATION


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